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UNIVERSITÉ DE MONTRÉAL

DESIGN ET TEST POUR LA HAUTE PERFORMANCE D'UN CONVERTISSEUR A/D BASÉ SUR L'ARCHITECTURE "SUBRANGING"

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THÈSE PRÉSENTÉE EN VUE DE L'OBTENTION

DU DIPLÔME DE PHILOSPHIAE DOCTOR (Ph. D.)

(GÉNIE ELECTRIQUE)

MARS 1998

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Cette thèse intitulée:

DESIGN ET TEST POUR LA HAUTE PERFORMANCE D'UN CONVERTISSEUR A/D BASÉ SUR L'ARCHITECTURE "SUBRANGING"

présenté par: EHSANIAN-MOFRAD Mehdi

en vue de l'obtention du diplôme de: Philosophiae Doctor

a été dûment acceptée par le jury d'examen constitué de:

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Je dédie cette thèse à mes parents, à ma femme, et à mes fils.

REMERCIEMENTS

Nous tenons à remercier ceux et celles qui, de près ou de loin, ont contribué à ce travail, dont:

Mme Bozena Kaminska, dont la direction a été fondamentale dans l'élaboration de cette thèse, le Département de Génie Électrique et de Génie Informatique de l'École Polytechnique de Montréal; Les membres du jury qui ont accepté d'évaluer le contenu de cette thèse dont M. Yvon Savaria, M. Mohammed Elmasry et M. Jean Jules Brault.;

Ma femme Elahe, mes fils Mohammed et Ahmad et l'ensemble de ma famille pour leur soutien, leurs encouragements et leurs prières tout au long de mes études; Naim Ben Hamida et Karim Arabi qui ont largement contribué à nos travaux et avec qui nous avons rédigé plusieurs articles dont deux décrits dans cette thèse; etc...

RÉSUMÉ

Un système de traitement numérique de données nécessite des circuits analogiques comme une interface entre le système numérique et le monde extérieur, qui a généralement un comportement analogique. Le convertisseur analogique-numérique joue un rôle significatif en agissant comme interface entre le monde extérieur et les systèmes numériques.

La précision, la vitesse et la dissipation de puissance sont les paramètres plus importants qui caractérisent les convertisseurs analogiques-numériques. Ces paramètres dépendent des techniques de conception des circuits, de l'architecture, et du mode d'opération des convertisseurs. Les convertisseurs analogiques-numériques de grande performance, sont généralement conçus en utilisant des architectures en pipeline et des techniques basées sur les condensateurs commutés. Cependant, le délai d'échantillonnage et le maintien (hold) entre les étages limitent la vitesse d'opération du convertisseur. En plus, la technologie de fabrication utilisée dans les circuits à base des capacités commutées n'est pas compatible avec la technologie de fabrication standard utilisée pour les circuits numériques. Notons aussi que la performance du convertisseur se dégrade lorsqu'il fonctionne sous de faibles tensions d'alimentation.

Afin de surmonter ces limitations, une nouvelle architecture de convertisseur analogique-numérique avec de nouvelles techniques de conception en mode tension a été proposée. Dans cette architecture, la vitesse de conversion a été améliorée par des opérations de soustraction et de comparaison exécutées en parallèle. Les sous-circuits de l'architecture proposée ont été conçus en utilisant une technologie BiCMOS à 0.8 μm. Ces sous-circuits forment un convertisseur de 3 bits suivi d'un convertisseur standard de 8 bits

dans le but de produire un convertisseur analogique-numérique de 11 bits. Dans notre première implantation, le convertisseur, dont le rapport signal sur bruit est de 62 dB pour une fréquence de 1 MHz, fonctionne avec une alimentation de 5 Volts. Nous avons trouvé que les erreurs de non-linéarité INL et DNL sont inférieures à 1 LSB pour un convertisseur de 11 bits.

L'opération sous de faibles tensions et la faible dissipation de puissance des circuits en mode courant, nous ont motivé à explorer une nouvelle architecture basée sur un fonctionnement en mode courant. Dans le but de concevoir un convertisseur analogique-numérique opérant en mode courant, le miroir de courant, qui est un composant fondamental de ce type de circuit, a été modélisé comme un interrupteur en mode courant. Ainsi, tous les paramètres d'un interrupteur normal ont été développés pour représenter un interrupteur en mode courant.

Un nouvel interrupteur en mode courant a été implanté en utilisant la technologie CMOS 1.2 µm de Mitel. Les résultats de test montrent que, pour certaines applications, les interrupteurs en mode courant peuvent avoir une meilleure performance que les interrupteurs en mode tension. Un commutateur dont la perte par insertion est de 0.7 dB à 300 MHz peut être un choix adéquat dans un convertisseur A/N en mode courant. Par conséquent, un convertisseur analogique-numérique de hautes performances de 12 bits est alors conçu par l'utilisation d'un commutateur en mode courant en vue d'une nouvelle architecture d'un convertisseur analogique-numérique. Cependant, ce convertisseur à 3 Volts montre des non-linéaritées INL et DNL de 1.5 et 1 bit respectivement. De plus, les performances du convertisseur A/N conçu montrent un rapport signal sur bruit de 60 dB pour un signal d'entrée de 100 KHz de fréquence et 10-bit comme nombre effectif de bits . Le nombre effectif de bits diminue à 9 quand la fréquence d'entrée augmente à 50 MHz.

Finalement, une nouvelle approche de test numérique a été explorée. Un BIST numérique a été conçu et appliqué pour les convertisseurs A/N. Le BIST est capable d'extraire les paramètres des convertisseurs A/N tels que le DNL, INL et les erreurs de décalage dans le domaine numérique. L'application d'un test dans le domaine numérique implique une augmentation de la précision du test. De plus, le BIST proposé permet d'éviter la méthode de calibration, ce qui conduit, par conséquent, à une réduction de la surface de silicium.

ABSTRACT

Complete digital signal processing requires analog circuits acting as interfaces between the digital system and the outside world, which is mostly analog. The analog-to-digital (A/D) converter plays a significant role as an interface between the physical world and digital systems.

Accuracy, speed and power dissipation are the main performance criteria for high speed analog-to-digital converters. These criteria depend on design techniques, architecture and mode of operation. A/D converters with a pipelined architecture and using switched-capacitance techniques are dominant in high performance analog-to-digital converters. However, the sample and hold delay between stages limits its speed. In addition, the technology used for switched-capacitor circuits is not compatible with standard digital process technology and their performances degrade at low voltage operation.

To overcome these limitations, a new architecture for A/D converters using some new design techniques has been explored in voltage mode. In this architecture, the conversion speed is improved by parallel subtraction and comparison. The subcircuits of this architecture have been designed in 0.8 μm BiCMOS technology. These subcircuits form a 3-bit converter followed by an 8-bit standard converter, which performs as an 11-bit analog-to-digital converter. In our first implementation, the A/D converter operates at 5 Volts and shows a signal-to-noise ratio of 62 dB at 1 MHz input frequency. The non-linearity errors, INL and DNL, are less than 1 LSB in the 11-bit A/D converter.

In addition, the low voltage and low power dissipation of current mode circuits motivated us to develop and explore the new architecture in current mode. In order to design

the current mode analog-to-digital converter, the current mirror, a fundamental circuit in current mode, has been modeled as a current mode switch. In this way, all the parameters of normal switches have been developed in a current mode switch. A novel current mode switch has been implemented in 1.2 μm CMOS MITEL technology. The test results show that the performance of current mode switches can be better than those of voltage mode switches for some applications. The low insertion loss of 0.7 dB at 300 MHz could make it a good candidate for a current mode A/D converter. A 12-bit high performance A/D converter has therefore been designed by applying current mode switch in a new A/D converter architecture. However, this 3-Volt converter shows INL and DNL non-linearity errors of 1.5 and 1 LSB respectively. In addition, the designed A/D has a 60 dB signal-to-noise ratio with 100 KHz input which shows 10 to 11 bits as the effective number of bits. The effective number of bits decreases to 9 when the input frequency increases to 50 MHz.

Finally, a new digital test approach has been investigated. A digital BIST has been designed and applied for a pipelined A/D converter. This BIST is capable of extracting in the digital domainA/D parameters such as DNL, INL, and offset errors . Applying a test in the digital domain increases test accuracy. In addition, the proposed BIST makes it possible to avoid calibration, which in turn reduces the area overhead.

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LISTE DES SIGLES ET ABRÉVIATIONS

A/D	Analog-to-digital
A/N	Analogique-numérique
BIST	Built in self-test
BCOM	Buffered inverter comparator
CAN	Convertisseurs analogiques-numériques
CMOS	Complementary MOS
CMFN	Common-mode feedback network
CNA	Convertisseur numérique-analogique
CCS	Controled current source
CLU	controled logic unit
CRU	Current read unit
CWU	Current write unit
D/A	Digital-to-analog
DMUX	Digital Multiplexer
DNL	Differential non-linearity
DR	Dynamic range

DSP	Digital signal processor
E/B	Échantilloneur-bloqueur
ENOB	Effective number of bits
FFT	Fast Fourier transform
FOM	Figure of merit
G_{err}	gain error
GBW	Gain-bandwidth
ICOM	Inverter comparator
INL	Integral non-linearity
Iss	Signal swing
LSB	Least significant bit
MOS	Metal-oxide semiconductor
MSB	Most significant bit
N/A	Numérique-analogique
P_{av}	Available power
P_{dis}	Power dissipation
P_{in}	Input power
P_{out}	Output power
O_{ffe}	Offset error

RF	Radio frequency
Ron	On resistance
r_{out}	Output resistance
SC	Switched-capacitor
S/H	Sample and hold
SI	Switched-current technique
SNR	Signal-to-noise ratio
SNRD	Signal-to-noise with distortion
SNWR	Signal-to-noise-without distortion ratio
SWI	Switch unit
THD	Total harmonic distortion
t_{on}	Turn on time
t_{off}	Turn off time
VLSI	Very large scale integration
V_{offe}	Offset voltage error
ω_{min}	Minimum bandwidth

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CHAPITRE I

Introduction

1.1 Motivation

La demande croissante des applications de traitement numérique de données, incluant les appareils vidéo portables, les appareils de communication, (e.g., les récepteurs sans-fil, les appareils magnétiques de stockage de données, etc, ont considérablement motivé les chercheurs à améliorer la performance des interfaces d'acquisition de données (voir la Figure 1.1). Aussi, l'augmentation considérable de la fréquence d'opération, de la densité des circuits intégrés, et le développement de nouvelles techniques de conception de circuits intégrés et de nouveaux algorithmes de traitement de données, ont conduit à la conception des processeurs numériques de signaux très performants. En effet, l'interface entre le monde physique, qui est généralement analogique, et les systèmes numériques limite encore la fréquence de fonctionnement et la précision d'acquisition des données. Parmi ces interfaces, on trouve les convertisseurs analogique-numérique (A/N) qui sont les plus difficiles à concevoir. Contrairement aux systèmes numériques, ces convertisseurs A/N ne peuvent atteindre une meilleure précision d'une manière arbitraire.

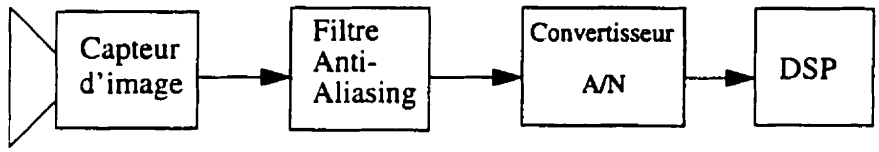
En effet, les nouvelles applications des convertisseurs A/N nécessitent de considérer certains facteurs clés tels que l'alimentation en tension, le mode de fonctionnement, la limitation de technologie et l'architecture. Le fonctionnement sous faible tension est le premier facteur en importance pour la conception des interfaces analogiques-numériques portables. La tendance actuelle est l'intégration des interfaces analogiques avec des cir-

cuits numériques pour former des circuits intégrés mixtes de grande complexité. Ces circuits mixtes contiennent en général de nombreux modules digitaux pour la partie de contrôle et le traitement des données ainsi qu'un ou deux blocs analogiques. L'utilisation de la même alimentation pour les deux circuits analogique et numérique est alors avantageuse, car elle permet de réduire le coût total du système. En effet, cela élimine le besoin de générer des sources d'alimentation multiples, qui sont souvent produites en utilisant des convertisseurs DC-DC. Par conséquent, pour être compatible avec des faibles tensions de fonctionnement du système, une nouvelle génération de convertisseurs analogique-numérique pouvant fonctionner avec une alimentation inférieure à 5V serait désirable.

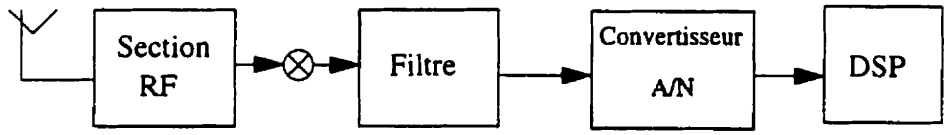
Le deuxième facteur clé est la limitation de la technologie et les techniques de conception. Plusieurs techniques ont été développées pour la conception et l'implantation de ces circuits analogiques. Ces techniques sont basées sur les condensateurs commutés. Cependant, ces techniques ne sont pas compatibles avec la conception et l'implantation d'un circuit mixte (analogique-numérique) nécessitant pour la partie analogique d'utiliser la même technologie que celle des circuits numériques. Cette intégration nécessite aussi que les deux types de circuits (analogique et numérique) utilisent la même source d'alimentation.

Les limitations de la technique basée sur les condensateurs commutés associées à la nécessité de disposer de condensateurs linéaires flottant et à la difficulté de réduire la tension d'alimentation, peuvent être réduites par la conception de convertisseurs en mode courant. Les circuits en mode courant, ou les circuits basés sur des courants commutés, (switched-current technique SI) sont des circuits analogiques à échantillonnage, dans lesquels les signaux sont représentés par des courants plutôt que par des tensions. La technique SI est basée sur une propriété des transistors MOS qui ont comme caractéristique de

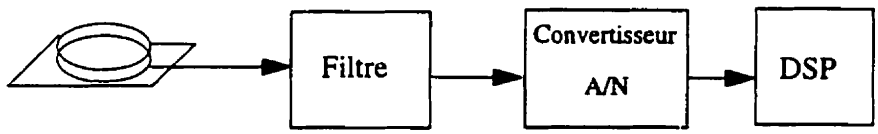
maintenir un courant de drain constant en fonction de la charge stockée dans la capacité de grille. Cela veut dire que les circuits SI n'ont pas besoin de condensateurs linéaires flottants, En d'autres termes, un procédé de fabrication double-poly n'est plus requis. Cette caractéristique rend les circuits SI compatibles avec les procédés standards pour le fabrication des circuits VLSI. De plus, puisque les circuits SI fonctionnent dans le domaine de courant, la tension d'alimentation peut être réduite.



(a) Système d'images vidéo



(b) Système de communication personnel



(c) Canal de lecture du lecteur de disquette

Figure 1.1 Exemples d'interfaces analogiques-numériques

Le troisième facteur clé est l'architecture du convertisseur A/N car cette dernière affecte la vitesse et la résolution du convertisseur A/N. Parmi les différentes architectures de convertisseurs A/N, les convertisseurs multi-pas sont les plus utilisés dans des applications à grande vitesse. Trois fonctions sont cruciales pour la réalisation de convertisseurs A/N multi-pas: la comparaison, la conversion (N/A) numérique-analogique et l'amplification. Dans les technologies CMOS, la précision avec laquelle ces fonctions peuvent être réalisées est limitée par le fait que le transistor MOS n'est pas un transistor idéal. Les effets qui accompagnent la réduction d'échelle (scaling) des dispositifs, sont l'appariement (matching) imparfait, l'impédance de sortie de valeur finie et la faible tension de claquage. Tous ces facteurs limitent les performances que peuvent atteindre ces fonctions, ce qui nécessite le recours à des techniques de calibration pour corriger de telles imperfections devenues trop importantes.

Dans les convertisseurs analogiques-numériques parallèles, la conception de comparateurs joue un rôle crucial dans la performance totale qui peut être atteinte. De plus, la vitesse, la résolution, l'impédance d'entrée, la dissipation de puissance, et la complexité d'un comparateur deviennent des facteurs de plus en plus importants lorsque le même comparateur est reproduit entre 50 à 100 fois ou plus dans une structure *flash*. La vitesse d'un comparateur est habituellement déterminée par le temps de recouvrement suite à une surcharge (*overload recovery)* de son pré-amplificateur, tandis que la résolution est souvent limitée par la tension de décalage de l'échantillonneur-bloqueur d'entrée. Pour une technologie donnée, il faut faire un compromis entre la vitesse du pré-amplificateur, le gain, la puissance dissipée, et la tension d'entrée. Si on peut trouver un moyen de réduire le décalage de l'échantillonneur-bloqueur, le pré-amplificateur peut être conçu pour un gain faible, ce qui permet d'obtenir un taux élevé de comparaison.

Pour transférer de l'information d'un étage à un autre pour une architecture multi-pas, des convertisseurs numériques-analogiques de grande précision sont requis. La non-linéarité et temps de stabilisation (settling) de ces convertisseurs contribuent directement à la distorsion harmonique et au délai du système numérique. Les convertisseurs numériques-analogiques (N/A) sont basés sur la subdivision des charges, du courant, ou de la tension, qui peuvent être implantés avec des matrices de capacités, des circuits de routage de courant (current-steering) ou avec des résistances variables. Ces différentes alternatives montrent plusieurs compromis à faire pour des technologies différentes. Ces alternatives doivent être analysées avec soin afin d'obtenir la meilleure performance possible.

Les convertisseurs analogique-numérique en pipeline contiennent souvent des étages intermédiaires pour relaxer la précision des étages subséquents. Quant ils sont implantés avec des condensateurs commutés dans une technologie CMOS, ces amplificateurs souffrent d'erreurs dans le gain dûs aux appariement imparfaits entre les capacités et au gain fini des amplificateurs opérationnels. Des techniques de calibration des capacités peuvent être utilisées pour réduire ces erreurs, mais ceci demande un grand choix de taille des capacités. Pour atteindre un gain d'une grande précision, d'autres méthodes de calibration doivent être utilisées. De plus, pour éliminer le besoin d'avoir un amplificateur opérationnel de grand gain, le processus de calibration doit inclure un amplificateur qui corrige le gain sans erreur.

Les limitations des architectures existantes demandent l'exploration de nouvelles architectures de convertisseurs analogique-numérique. Ces architectures doivent être considérées au niveau circuit, au niveau système et au niveau technologie. Le mode de fonctionnement et le test des convertisseurs doivent être pris en considération.

1.2 Objectifs de la thèse

L'objectif principal de cette thèse est de développer, concevoir et tester un convertisseur analogique-numérique de grande performance. Différentes techniques doivent être examinées afin d'atteindre cet objectif. Pour l'atteindre, nous avons concentré nos efforts sur les champs de recherche suivants.

[1] *Explorer une nouvelle architecture de convertisseur A/N basée sur une nouvelle technique de le "subranging"*. Dans cette conception, la vitesse de conversion a été améliorée par la comparaison et la soustraction en parallèle.

[2] La conception et l'implantation d'une nouvelle architecture en mode tension. L'architecture que nous proposons a été développée en utilisant la technologie 0.8 µm BiCMOS. Le convertisseur exécute une conversion de 3-bit ou de 4-bit, suivie d'une conversion flash standard, comme, par exemple, pour un convertisseur de 8-bits. La première cellule doit être minutieusement conçue pour minimiser les erreurs dans le convertisseur numérique-analogique (A/N) au complet. Ceci nécessite le développement de nouveaux circuits qui peuvent s'adapter avec la nouvelle architecture du convertisseur A/N. Dans cette architecture, un nouvel amplificateur opérationnel BiCMOS a été conçu et testé pour faire la soustraction. Dans notre première implantation, le convertisseur analogique-numérique A/N fonctionne à une fréquence de 1 MHz avec un rapport signal sur bruit de 62 dB. Les erreurs de non-linéarité INL et DNL ont été inférieures à 1 LSB pour un convertisseur A/N de 11-bits. Les résultats montrent la possibilité d'augmenter la résolution de 3-bit pour n'importe quel convertisseur. Donc, un étage pour le prétraitement est proposé pour augmenter la résolution pour n'importe quel convertisseur.

[3] *la conception et l'implantation de la nouvelle architecture en mode courant.* Ici, l'architecture a été conçue en mode courant avec quelques modifications dans l'architecture du convertisseur. L'objectif est d'examiner l'architecture proposée de sorte qu'elle puisse fonctionner avec une faible tension et peut être intégrée dans les circuits numériques sans en changer la technologie. La nouvelle architecture montre un potentiel important pour des convertisseurs fonctionnant à de faibles tensions et de grandes performances. Dans cette conception, une technique numérique de correction d'erreurs a été utilisée pour réduire l'erreur de décalage des comparateurs. Le circuit a été implanté en technologie MITEL CMOS 1.2 µm MITEL.

[4] *Analyse et conception du mode commutation de courant pour des applications en mode courant.* Dans la plupart des circuits basés sur le mode courant, les mémoires de courant jouent un rôle primordial dans la précision des circuits. Dans cette section, la mémoire de courant a été examinée d'un nouveau point de vue. Ces mémoires ont été caractérisées par des paramètres ordinaires comme la perte d'insertion et d'isolation. Cette nouvelle manière de caractériser des mémoires de courant peut nous aider à appliquer les mêmes outils d'analyse utilisés en mode tension pour les circuits en mode courant. Pour vérifier la commutation mode-courant, nous avons réalisé un circuit qui a été testé en utilisant la technologie CMOS 1.2 µm MITEL. Les résultats des tests montrent que les commutateurs mode courant peuvent avoir de meilleures performances que les commutations mode tension pour certaines applications. Nous sommes arrivés à la conclusion que la commutation mode courant avec une faible perte d'insertion (insertion loss) de 0.7 dB peut être facilement utilisée dans les convertisseurs analogiques en mode courant.

[5] *La conception d'un circuit d'auto test (BIST).* Une nouvelle approche de test a été examinée dans cette partie. Ce circuit BIST a été conçu et utilisé avec un convertisseur A/N en pipeline. Ce BIST est capable d'extraire des paramètres d'un convertisseur tel que le DNL, l'INL, et l'erreur de décalage dans le domaine digital. Appliquer un test dans le domaine numérique a comme effet d'augmenter la précision du test. En plus, le BIST proposé élimine la nécessité de recourir à une méthode de calibration. Ceci a pour effet de réduire la surface additionnelle.

1.3 Organisation de la thèse

Cette thèse est constituée de sept chapitres. Le Chapitre 2 décrit plusieurs types d'architectures de convertisseurs analogique-numérique A/N avec une attention particulière à leur réalisation dans des technologies VLSI. Les limitations de ces architectures sont aussi étudiées selon les exigences des fonctions suivantes: comparaison, conversion numérique-analogique (N/A), et soustraction.

Dans le Chapitre 3, nous décrirons la conception d'un convertisseur 11-bit 1-MHz en utilisant la technologie BiCMOS. Ici, la conception d'un amplificateur opérationnel avec la technique de compensation "feedforward" est présentée. L'amplificateur opérationnel fonctionne à 900MHz GBW avec un gain DC de 90 dB. Ce chapitre montre aussi la conception de l'auto-calibration du comparateur BiCMOS avec une tension de décalage de 200 μV. Ensuite, les performances des convertisseurs A/N sont analysées avec ces circuits.

Le chapitre 4 discute de la conception de commutateur en mode courant. Les résultats expérimentaux et les résultats de simulation appuient la discussion.

Au chapitre 5, nous présenterons la conception de convertisseur analogique-numérique en mode courant. Dans ce chapitre, nous examinerons un convertisseur A/N en mode courant de 12 bits de résolution. Les sources d'erreurs ont été analysées en profondeur. La conception et l'analyse sont supportées par des résultats de simulation.

Au Chapitre 6, nous présenterons et nous discuterons la conception d'un circuit d'auto test (BIST) pour les convertisseurs analogique-numérique.

Finalement, nous conclurons au Chapitre 7.

CHAPITRE II

Les architectures des convertisseurs A/N

2.1 Introduction

La conception de nouveaux convertisseurs analogiques-numériques (CAN) requiert de nouvelles architectures ainsi que de nouvelles techniques de conception de circuit. Le choix d'une architecture dépend des performances des blocs principaux, de la technologie de fabrication et bien sur de l'application visée.

Ce chapitre consiste en une revue générale des architectures des CANs en décrivant leur performance en technologies CMOS et BiCMOS. Ces architectures sont classées en deux catégories principales: les CANs de taux de Nyquist et les CANs Sigma-Delta. Les CANs de taux de Nyquist sont à leur tour classifiés en deux catégories: les CAN à une étape comme l'architecture *flash* et les CAN à multi-étapes tel que *subranging* et les approximation successive. Les effets sur les performances des CAN des fonctions de base tel que la comparaison, la conversion analogique numérique, la soustraction et l'échantillonnage seront discutés dans ce chapitre.

2.2 Les paramètres des performances

Dans cette section, on définit quelques paramètres qui serviront à la comparaison des différentes architectures. La plupart de ces définitions sont présentées dans la littérature [1], [2]. La Figure 2.1 montre graphiquement certaines de ces définitions.

- La non-linéarité différentielle (DNL) est définie comme étant la déviation maximale de la largeur du pas de l'axe de l'entrée par rapport à la valeur idéale du bit le moins significatif (LSB).
- La non-linéarité intégrale (INL) est la déviation maximale de la caractéristique entrée/sortie par rapport à la ligne droite reliant les deux bouts.
- L'erreur de décalage est le décalage horizontal dans la caractéristique de transfert idéale du CAN.
- L'erreur du gain est la différence entre les valeurs idéales et réelles de la caractéristique de transfert quand le décalage est nul.

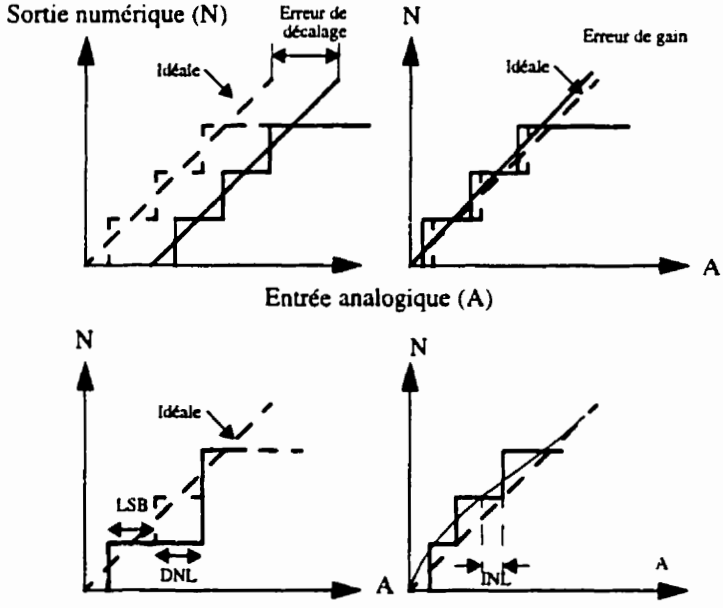


Figure 2.1 Définition des erreurs statiques dans les CAN.

Les définitions mentionnées ci-haut décrivent le comportement statique des CAN. Plusieurs termes sont souvent utilisés pour décrire le comportement dynamique des convertisseurs.

- Le rapport signal sur bruit (SNR) est défini comme étant le rapport de la puissance du signal par rapport à celle du bruit de quantification à la sortie.
- Le rapport signal-(bruit+distorsion) (SNRD) est le rapport de la puissance du signal par rapport au bruit total et la distorsion harmonique à la sortie quand l'entrée est sinusoïdale.
- La marge dynamique (DR) du convertisseur sans bruit est le rapport du pleine échelle par rapport à la plus petite différence que le CAN peut distinguer. Si la puissance du bruit est indépendante de l'amplitude du signal, la DR est égale au SNR à la pleine échelle. Cependant, dans les cas où la puissance du bruit augmente avec le niveau du signal, le SNR maximum est inférieur à la DR.
- La marge dynamique libre est le rapport du niveau du signal d'entrée au SNRD maximum sur celui au SNRD= 0dB. Cette mesure de la DR est utile car elle indique la valeur de la DR avant que la distorsion ne domine le bruit. La Figure 2.2 montre comment déterminer la marge dynamique libre et la marge dynamique à partir de la courbe SNRD en fonction du niveau d'entrée.
- Le temps de recouvrement suite à une surcharge est le temps requis par le circuit pour revenir à son opération linéaire après la suppression de l'entrée qui a poussé le circuit à la saturation à cause de son amplitude élevée.

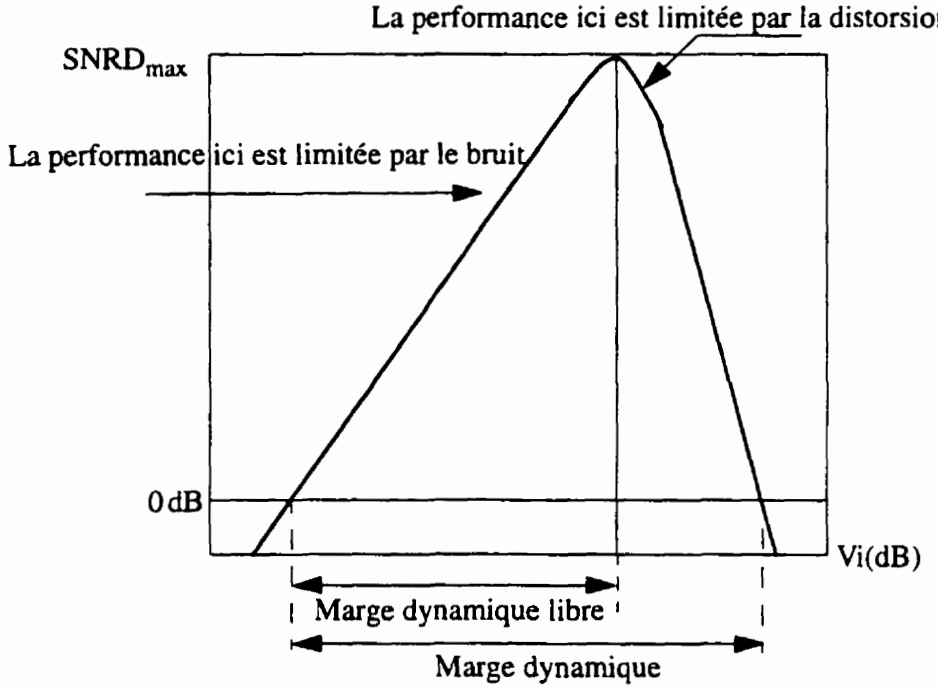


Figure 2.2 SNRD en fonction du niveau du signal dans un CAN.

2.3 Le CAN flash

Le CAN flash est une architecture complète qui se caractérise par un parallélisme maximum et une vitesse maximale durant l'étape de la conversion. Le schéma bloc d'un CAN flash à M-bit est présenté à la Figure 2.3. Les 2^M comparateurs sont utilisés pour comparer le signal d'entrée aux 2^M tensions de référence (Vref). L'avantage principal du CAN flash est que la conversion se fait en une seule étape. Donc, aucun post-traitement analogique n'est nécessaire comme la conversion numérique-analogique ou bien la soustraction. En plus, le codage numérique pourrait être pipeliné pour améliorer la vitesse et réduire les erreurs de stabilité [3].

Malgré ses avantages, le convertisseur flash a des inconvénients qui limitent son application en haute fréquence et dans la conversion à haute précision. Ces limitations sont la différence des délais entre les comparateurs, la capacité d'entrée non-linéaire et la dépendance exponentielle de la puissance et la surface de nombre de bits. Des techniques comme le repliement[4] et le moyennage [5] ont été proposés pour surmonter quelques limitations.

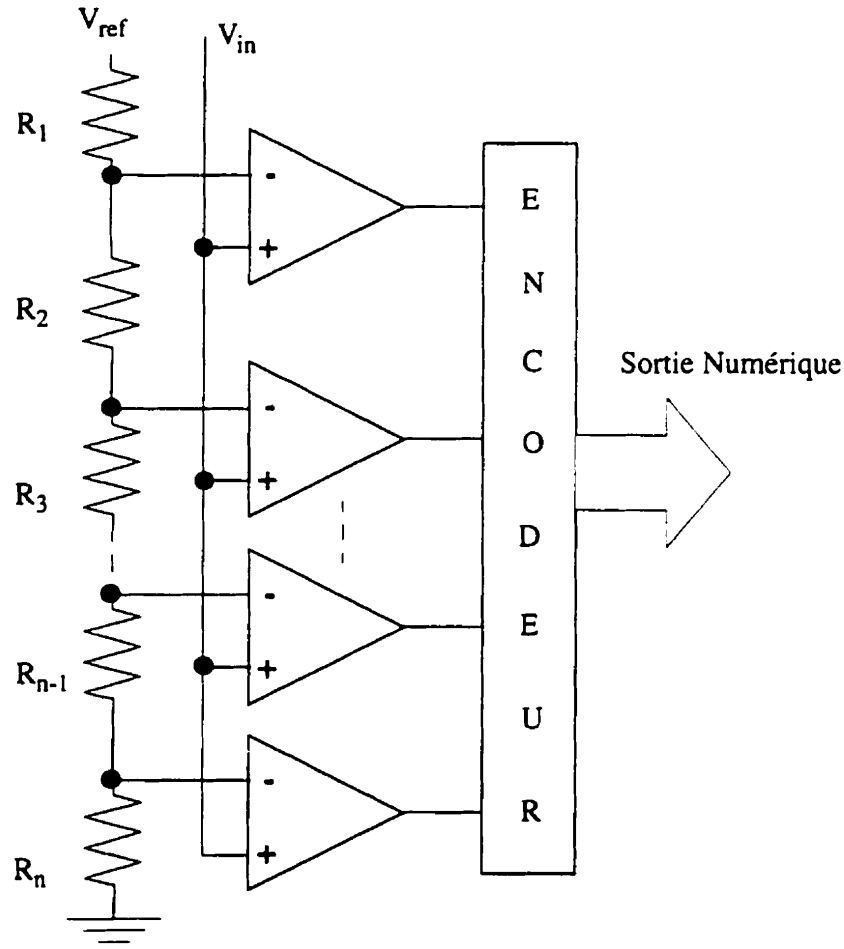


Figure 2.3 L'architecture du CAN Flash.

La vitesse et la précision du CAN flash dépendent des comparateurs et de la technologie utilisée. Les composants CMOS ont une faible transconductance, ce qui cause un long

délai et un long temps de recouvrement suite à une surcharge. De plus, les appariements imparfaits forcent l'introduction d'un circuit d'annulation de décalage. En plus, les différences de délais des comparateurs requièrent l'utilisation d'un circuit échantillonneur-bloqueur à l'entrée. Vue ces limitations, la technologie CMOS n'est donc pas idéale pour réaliser des CAN rapides. C'est la technologie bipolaire qui est surtout utilisée pour des conversions flash dû à sa haute vitesse et à ses meilleures appariements.

En résumé, le CAN flash est choisi pour des applications à haute vitesse et à résolution modérée. Cependant, les erreurs dynamiques et statiques, la dissipation de puissance et les capacités d'entrée limitent l'utilisation pratique de cette architecture pour des résolution inférieure à 10 bits.

2.4 CAN à deux étapes

L'architecture multi-étape est conçue pour surmonter les inconvénients de l'architecture flash. L'opération de base de l'architecture à deux-étapes est de faire une conversion approximative qui fournit une estimation de l'entrée, suivie d'une conversion précise pour numériser la différence entre l'entrée et sa valeur estimée. Cette architecture est présentée à la Figure 2.4. Elle consiste en un CAN flash, un convertisseur numérique-analogique (CNA), un soustracteur et un CAN flash précis.

L'avantage principal du CAN à deux-étapes est que sa dissipation de puissance et sa surface sont proportionnelles à $2^{M/2}$ pour un convertisseur M-bit comparé à 2^{M} pour l'architecture flash. Les inconvénients de cette architecture sont que:

- Sa vitesse est deux fois plus petite que celle de l'architecture flash.

- Le CNA utilisé dans cette architecture doit avoir une linéarité intégrale au moins égale à celle du système. Cette exigence cause un délai additionnel réduisant ainsi la vitesse de conversion.
- Le délai entre le premier et le deuxième étage requiert l'utilisation d'un échantillonneur-bloqueur (E/B) explicite qui, à son tour, requiert un amplificateur opérationnel à gain et marge de sortie assez élevés.
- Cette structure requiert un soustracteur à boucle fermée explicite qui, à son tour, contribue au délai et réduit la vitesse.

Le potentiel de l'architecture à deux-étapes a été démontré par l'implantation d'un CAN bipolaire 10-bit, 75-MHz [6] et 12-bit 1-MHz CMOS [10]. Les performances des circuits bipolaires se dégradent en haute résolution ce qui rend la calibration difficile. D'autre part, les circuits CMOS peuvent utiliser une méthode d'auto-calibration pour atteindre des résolutions élevées. Cependant, les circuits BiCMOS peuvent améliorer les performances.

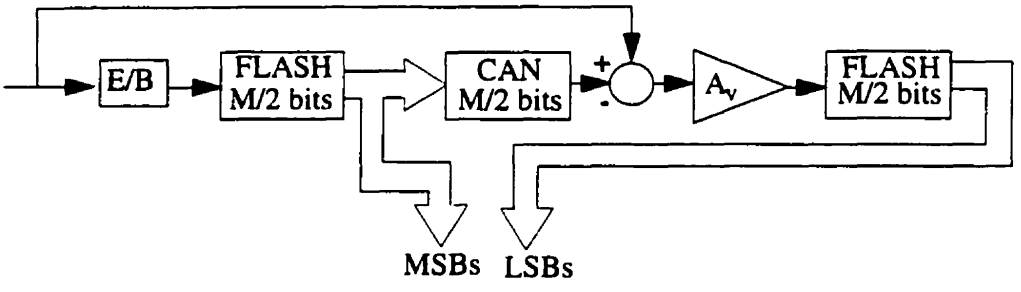


Figure 2.4 L'architecture du CAN à deux étapes.

Un convertisseur CAN à deux étapes n'a pas nécessairement besoin de deux étages; un étage flash peut réaliser les deux conversions approximatives et précises. Ce concept, appelé le recyclage [7], réduit la surface du dé et la dissipation de puissance, mais il impose au design d'autres limitations comme l'utilisation de comparateurs à faible décalage ou bien de soustracteurs à gain élevé, qui, par leur participation au délai, réduisent la vitesse globale.

L'architecture "subranging", une classe des CAN à deux étapes, élimine le besoin d'un soustracteur explicite. Cette architecture consiste en deux parties. La première est un étage flash approximatif et la deuxième est un étage flash précis. La tension de référence dans le deuxième étage est une subdivision de la première tension de référence qui est proche de l'entrée [11]. Une description complète d'une variété de l'architecture "subranging" sera discutée dans le chapitre 5. Donc, l'architecture "subranging" empêche le traitement linéaire entre les étages en éliminant les soustracteurs. Cependant, elle fait face à d'autre difficultés dans la deuxième tension de référence et le comparateur qui dégradent la vitesse du CAN.

En résumé, l'architecture à deux étapes est un choix viable pour la réalisation des circuits de CAN VLSI fonctionnant à des fréquences vidéo (5-100 MHz).

2.5 Les CAN pipelinés

Le concept du pipelinage peut être appliqué dans le domaine analogique pour réaliser des vitesses élevées à travers les opérations concurrentes [5]. La Figure 2.4 présente un diagramme bloc du CAN pipeliné. Il consiste en K étages, dont chacun contient un circuit échantionneur bloqueur (E/B), un CAN, un soustracteur, un CNA et un amplificateur. Le premier étage échantillonne et bloque l'entrée analogique et produit une estimation numérique de l'entrée de M-bit. Ensuite, il convertit l'estimation en analogique et la soustrait de

l'entrée bloquée. Si on suppose que le CNA et le CAN flash sont réalisés, la tension résiduelle est entre 0 et $Vref/2^M$. Donc, dans l'architecture pipelinée, une amplification de la tension résiduelle par 2^M est nécessaire pour que le convertisseur flash dans l'étage suivant puisse être utilisé avec la même tension de référence. Le deuxième étage dans le pipeline échantillonne la tension résiduelle et réalise la même séquence d'opérations. Ceci est répété dans tous les étages suivants. Du moment que chaque étage réalise la fonction d'échantillonnage et de maintien, permettant aux différents étages de réaliser simultanément différents échantillonnages. Dans ce cas, le temps de conversion dépend du temps de stabilisation d'un seul étage. La surface du convertisseur pipeline augmente linéairement avec l'augmentation de la résolution, contrairement à un flash, où l'augmentation est exponentielle.

Les erreurs qui peuvent limiter les performances des CAN pipelinés sont: les erreurs de décalage dans les circuits E/B et les amplificateurs, les erreurs de gain dans les amplificateurs des circuits E/B, la non-linéarité des sous-convertisseurs analogiques-numériques, la non-linéarité des sous-convertisseurs numériques-analogiques et le temps du stabilisation des amplificateurs opérationnels.

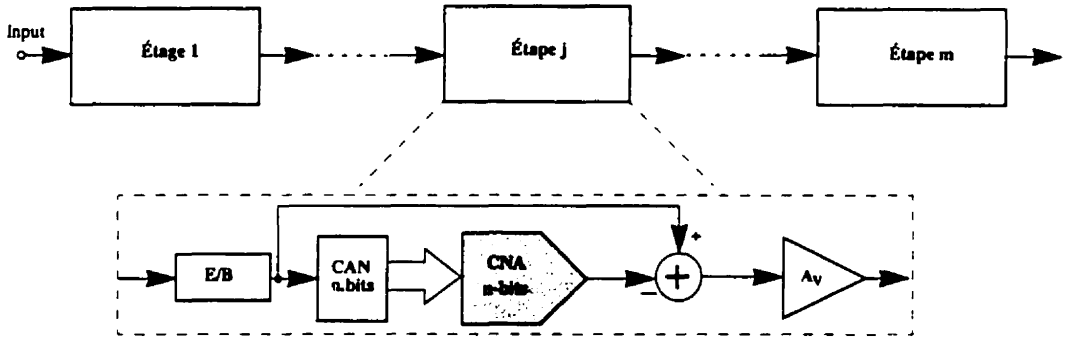


Figure 2.5 L'architecture du CAN pipeliné.

L'architecture pipeline dépend fortement des performances des amplificateurs opérationnels utilisés dans les circuits E/B et les amplificateurs inter-étages. Les amplificateurs opérationnels à gain élevé et marge de tension de sortie élevée souffrent d'une dégradation de leur taux de changement de la sortie (slew rate) et de la marge de phase. L'implantation pratique de l'architecture pipelinée peut se faire sous plusieurs configurations: des étages flash en cascade [9] ou bien des étages à un bit.

En résumé, avec ses opérations concurrentes, l'architecture pipelinée est adoptée pour la conversion à haute vitesse. Elle doit par contre faire face à un compromis dans la conception des amplificateurs opérationnels.

2.6 CAN à approximation successive

La Figure 2.5 illustre le CAN à approximation successive. Ce convertisseur consiste en un comparateur, un CNA et une unité numérique de contrôle logique. La fonction de cette dernière est de déterminer la valeur de chaque bit d'une manière séquentielle basée sur la sortie du comparateur. Dans chaque cycle, le circuit divise la différence entre le signal échantilloné et la sortie du CNA. Ceci est réalisé en détectant la polarité de la différence et en changeant la sortie du CNA dans la direction qui réduit cette différence. La conversion requiert au moins N cycles d'horloge pour obtenir une résolution de N-bit.

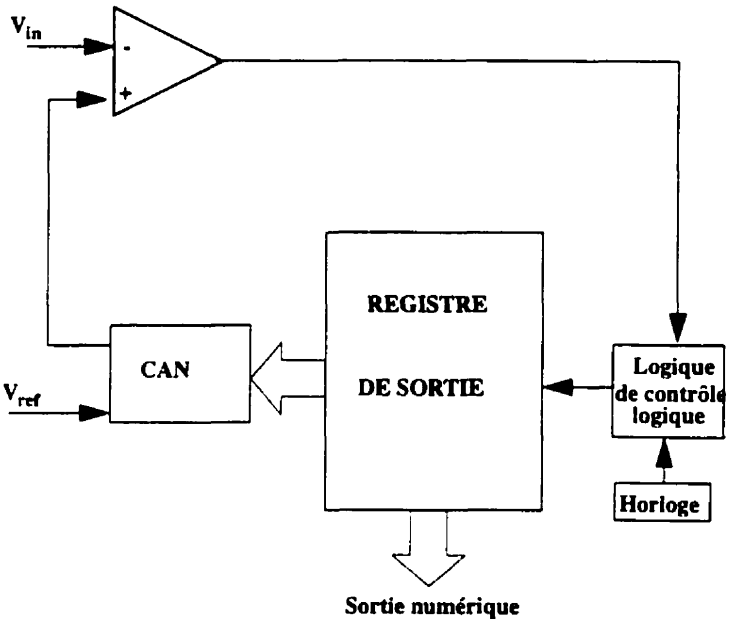


Figure 2.6 L'architecture du CAN à approximation successive.

Les erreurs de non-linéarité différentielle et intégrale de cette technique dépendent seulement du CNA. Cependant, le CNA est le seul élément dans cette architecture qui doit être implanté avec précision.

2.7 CAN à sur-échantillonnage

Les CANs à sur-échantillonnage basés sur le modulateur sigma-delta sont souvent utilisés dans les systèmes d'acquisition de signal à haute résolution. Les applications suivantes sont un exemple: télécommunications (bande vocale), audio numérique et ISDN. Les fréquences peuvent atteindre quelques MHz.

Le filtre passe-bas à l'entrée du CAN conventionnel atténue le bruit des hautes fréquences et les composantes hors-bande du signal qui se replient sur le signal après l'échan-

tillonnage à la fréquence de Nyquist. Les caractéristiques de ce filtre est normalement spécifiées pour chaque application.

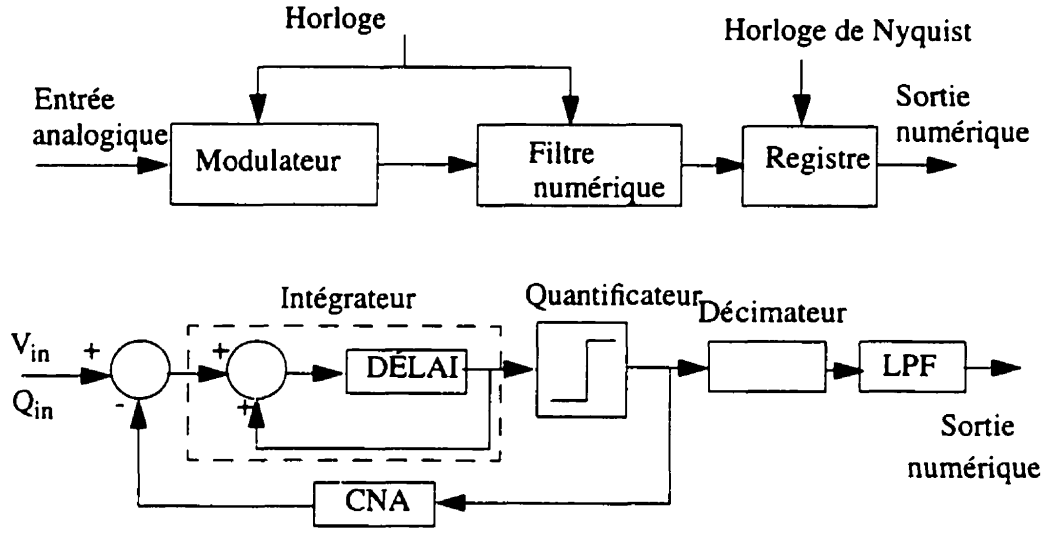


Figure 2.7 L'architecture du CAN à sur-échantillonnage.

Les convertisseurs à sur-échantillonnage, illustrés à la Figure 2.7, peuvent utiliser des composants analogiques simples et à faible précision, mais ils requièrent des étages de traitement numériques rapides et complexes. Ils modulent l'entrée analogique avec un code numérique simple, souvent des mots de 1 bit, à une fréquence supérieure à celle de Nyquist. Il est démontré que la conception du modulateur est un compromis entre la résolution en temps et la résolution en amplitude d'une façon que des circuits analogiques imprécis puissent être utilisés. L'utilisation d'un modulateur à haute fréquence élimine le besoin des filtres abruptes à l'entrée du CAN. Un filtre numérique à la sortie élimine le bruit, l'interférence et les composants haute fréquence du signal avant qu'elles se replient sur le signal quand le code est ré-échantillonné à la fréquence de Nyquist.

2.8 Performances récentes atteintes avec des CANs

Dans cette section, des résultats publiés sur les CANs à haute résolution sont comparés. La Tableau 2.1 présente les principales performances de chaque CAN. Quand la résolution augmente, la dissipation de puissance augmente car le nombre de composants utilisés augmente. On suppose aussi que la puissance dans les CANs augmente linéairement avec la fréquence d'échantillonnage et la longueur de canal minimum disponible. En réalité, la dissipation de puissance devient non-linéaire quand les possibilités en vitesse du procédé technologique sont poussées aux limites. De plus, les CANs sont composés de différents circuits dont les tailles changent différemment avec le procédé. De ce tableau, on constate que les CAN à sur-échantillonnage dominent dans les applications à haute résolution. Cependant, les pipelines sont les plus efficaces. De plus, la résolution des convertisseurs pipelines s'est améliorée et ces derniers sont devenus compétitifs avec les convertisseurs à sur-échantillonnage.

Tableau 2.1 Performances récentes des CANs

Réf	Année	Tech	Tension d'alimentation	DR (bit)	SNDR dB	Taux d'chan (MHz)	Puissance (mW)	Architecture
[R8]	91	3 um CMOS	5	13	72	2.5	100	pipeline
[22]	91	2 um BiCMOS	10	10	55	20	1000	Pipeline
[21]	92	1 um CMOS	5	12	65	5	200	Falsh 2-Étage
[23]	94	1.2 um BiCMOS	5	16	97	0.04	180	Sigma delta
[18]	92	0.9 um CMOS		10	60	20	240	pipeline
[12]	91	1 um CMOS	5	12	74	2.1	41	Sigma delta
[19]	91	2 um BiCMOS	10	12	73	1.25	600	Successive

Tableau 2.1 Performances récentes des CANs

Réf	Année	Tech	Tension d'alimentation	DR (bit)	SNDR dB	Taux d'chan (MHz)	Puissance (mW)	Architecture
[16]	93	2.4 um BiCMOS	8	15	79	1	1800	pipeline
[15]	93	1 um CMOS	5	15	89	0.048	100	Sigma delta
[26]	93	0.8 um CMOS	5	10	53	50	900	pipeline
[25]	93	0.8 um BiCMOS	5	10	55	0.5	20	Pipeline
[14]	93	Bipolar	10	10	59	75	800	Pipeline
[17]	93	0.8 um CMOS	2.5	10	55	20	30	Pipeline
[20]	95	0.8 um CMOS	2.7	10	54	40	85	Pipeline
[13]	94	1.2 um CMOS	3.3	10	59.1	20	35	Pipeline
[24]	94	0.8 um CMOS	3	12		1	1	Succes-sive

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CHAPITRE III

Un nouveau convertisseur A/N pour des applications à haute résolution et haute vitesse

3.1 Résumé

Dans les chapitres précédents, on a démontré que les convertisseurs analogiques-numériques constituent le lien entre le monde analogique et les systèmes numériques. Ils apparaissent comme le goulot des systèmes de traitement de données qui réalisent des opérations analogiques et mixtes (analogiques et numériques). Ce goulot limite donc la vitesse et la précision des systèmes. Traditionnellement, les CAN rapides utilisent l'architecture flash parallèle tel que mentionné au chapitre 2. Cependant, la plupart des circuits intégrés sont incapables de convertir, avec une précision élevée, des signaux de haute amplitude et de haute fréquence pour un traitement de signal de haute performance. Ces convertisseurs introduisent une dégradation de plus que 24 dB du rapport signal sur bruit plus le rapport de distorsion à la fréquence de Nyquist par rapport aux caractéristiques à basse fréquence. Cette dégradation est causée par les différences des délais du signal dans le circuit et la non-linéarité des capacités d'entrée.

En même temps, les CANs "subranging" offrent des performances qui sont difficilement atteignable par les CANs flash ou à approximation successive. Ils peuvent fournir des conversions rapides et très précises. Le CAN "subranging" conventionnel, qui consiste

en deux divisions de référence consécutives, est souvent réalisé avec des chaînes de résistances et des interrupteurs Ceci peut être vu comme une conversion N/A. Alors qu'ils évitent les délais des soustractions, ce type de CAN se confronte à d'autres difficultés dans la réalisation de CNA et la conception des comparateurs qui peuvent en dégrader considérablement la vitesse.

Ce chapitre décrit une nouvelle architecture "subranging" pour les CANs pour des applications de hautes performances. Un convertisseur à haute vitesse et haute résolution a été réalisé en combinant les opérations de soustraction et de comparaison. Le convertisseur réalise une conversion de 3 bits suivie par une conversion flash standard, de 8 bits par exemple. La première cellule de 3 bits a été conçue minutieusement dans le but de minimiser les erreurs dans le CAN. Cette cellule consiste surtout en des comparateurs et un soustracteur. Le soustracteur utilise un amplificateur opérationnel offrant un produit gain - largeur de bande de 900 MHz. Un comparateur d'autocalibration, à haute vitesse et faible décalage est utilisé dans la cellule qui fonctionne à 200 MHz. Ces circuits sont conçus en technologie BiCMOS 0.8 µm. Dans notre implantation, le CAN fonctionne à 1 MHz avec un rapport signal sur bruit de 62 dB. Les erreurs de non-linéarité, INL et DNL, sont de moins de 1 LSB dans le CAN à 11-bit. Les résultats montrent la possibilité d'augmenter la résolution de n'importe quel CAN de 3 bits. Donc, un étage de pré-traitement est proposé pour l'amélioration de la résolution. Avec cette technique, un CAN à résolution supérieure à 15 bits devient possible.

Dans la deuxième partie de ce chapitre, une revue des différentes architectures du CAN à "subranging" est présentée. La nouvelle architecture "subranging" est présentée dans la troisième partie. Les performances des sous-circuits et les considérations relatives à la conception sont discutées dans la quatrième partie. Enfin, les performances du sys-

tème et les résultats expérimentaux font l'objet de la dernière partie. Notons que l'article proposé dans ce chapitre a été soumis au "Journal of Analog Integrated Circuits and Signal Processing".

A Novel A/D Converter For High Resolution and High Speed Applications

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Note: This paper has been submitted for publication in the Journal of Analog Integrated Circuits and Signal Processing, Kluwer Publishing.

3.2 Abstract

This paper describes a new subranging architecture for analog-to-digital converters for high performance applications. A high-resolution and high-speed converter has been achieved as a result of performing subtraction and comparison operations simultaneously. The converter performs a 3-bit conversion followed by a standard flash conversion, 8-bit for instance The first 3-bit cell has been designed in order to minimize the errors in the A/D converter. This cell mainly consists of comparators and a subtracter. The subtracter employs a high gain-bandwidth operational amplifier, 900 MHz gain-bandwidth(GBW). A high-speed and low-offset comparator using a self-calibrating technique is used in the cell which operates at 200 MHz. These circuits are designed in 0.8 µm BiCMOS technology. In our implementation, the A/D converter operates at input frequency of 1 MHz with a signal-to-noise ratio of 62 dB. The non-linearity errors, INL and DNL, are less than 1 LSB in the 11-bit A/D converter. The results show the possibility of increasing the resolution of any converter by 3 bits.

3.3 Introduction

Analog-to-digital(A/D) converters provide the link between the analog world and digital systems. Due to the extensive use of analog and mixed analog-digital operations, A/D converters often appear as the bottleneck in data processing applications, limiting overall speed or precision. Traditional designs of high-speed A/D converters have used a fully parallel flash architecture. However, most ICs are unable to convert large-amplitude high-frequency analog input signals with a sufficient resolution for high-performance signal processing. These converters suffer degradation of more than 24 dB of signal-to-noise ratio[8] and distortion ratio at the Nyquist frequency compared to the characteristics at low input frequency. This degradation is caused by signal delay differences in a circuit and non-linearity of input capacitances [6], [1].

At the same time, subranging A/D converters offer performance levels which are difficult to obtain with the successive-approximation or flash converter architecture. They can deliver high conversion speed and resolution. The conventional subranging A/D converter, which consists of two consecutive reference divisions, is usually realized with resistor ladders and switches. This can be viewed as a D/A conversion function. While avoiding the delay associated with subtraction, such a converter must cope with other difficulties in D/A converter and comparator design which may substantially degrade its speed [13].

Silicon bipolar technology has traditionally dominated the field of high-speed data conversion circuits. However, the emergence of BiCMOS as a viable mainstream VLSI technology offers new opportunities for improving the performance of such circuits by combining the complementary advantages of each technology. Relative to MOS devices, bipolar transistors exhibit superior threshold matching, higher transconductance, and

lower noise levels. These attributes make bipolar circuits especially well-suited to providing low-noise amplification over large bandwidths. Altenatively, CMOS technology provides the substantial advantages of simple zero-offset, low leakage analog switches, high-impedance charge storage nodes, and complementary devices. These CMOS characteristics allow for the extensive use of analog sampling and pipelining. Through the selective use of these attributes, BiCMOS technology offers the potential of significant performance improvements in a wide variety of circuit application, including the design of comparator and subtracter in the proposed subranging A/D converter.

This paper presents a novel architecture for a subranging A/D converter suitable for high frequency and high resolution applications. The need for sample and hold circuits, which limit the conversion rate in all multi-stage A/D converters, can be eliminated by careful design. The speed is enhanced by performing the comparison and subtraction operation simultaneously. The new subranging A/D converter comprises two stages. The first stage includes a 3-bit subranging cell which determines the accuracy and speed of the entire A/D converter. The second stage can employ any standard flash A/D converter. An 8-bit converter will be used here.

In the second part of this paper, the various architectures of subranging A/D converters are reviewed. The new subranging architecture is described in the third part. The performance of subcircuits and their design considerations are discussed in the fourth part. System performance and experimental results are presented in the last part.

3.4 Design Problems in Large Bandwidth A/D Converters

3.4.1 Timing Accuracy

There are two main problems that degrade the dynamic performance of high-speed A/D converters: timing inaccuracies and distortion. If the input signal changes with the slew rate of S, then

$$\frac{dX}{dT} > S \tag{3.1}$$

where dX and dT are the accuracies of signal and time for a signal X at time T. Thus, for a full-scale analog input $X = A \sin 2\pi ft$, whose maximum rate of change is equal to $2\pi fA$, the above condition can be expressed as

$$2\pi f_{in} A \cdot dT < 1LSB \tag{3.2}$$

If the full-scale range is twice the amplitude of the signal and $LSB = 2A / 2^N$, then

$$dT < \frac{2^{-N}}{\pi f_{in}} \tag{3.3}$$

Evaluating this expression for an 11-bit converter with a maximum analog input frequency of 10 MHz results in a maximum timing error of 16 ps. The same expression for a 3-bit converter with an input frequency of 1MHz gives 50 ns. This timing error imposes some limitations on the design and layout of converters.

Timing error is generated by three kinds of error sources:jitter, skew of the clock and input signal at different places on the chip, and signal-dependent delay. The sampling clock jitter can originate both inside and outside the A/D converter. The outside sampling clock must be designed to have a very small short-term jitter. Internally, a small rise or fall time of the sampling clock avoids jitter caused by white noise of the clock amplifier cir-

cuits. Furthermore, crosstalk from other circuits must be minimized to avoid modulation of the sampling clock.

The skew between the clock and the analog signal introduces timing errors in the same signal at different places on the die. The clock signal at the top comparator stage, for example, may be slightly out of phase with the clock signal at the middle comparator. This difference in time causes a quantization error which results in non-linear distortions. Thus, the sampling clock lines and the signal lines in the converter must be laid out very carefully.

Finally, many circuits introduce signal-dependent delays. Comparators, which consist of amplitude limiting circuit followed by a bandwidth limiting circuit, are the main sources of this error.

3.4.2 Distortion

The quantized signal can be distorted by three sources: large aperture time of the sampling comparator, distortion in the linear part of the input amplifier and the comparator input circuits, and changes in the reference voltage values.

A large comparator aperture time may be caused by the architecture of the comparator or by a large rise or fall time of the sampling clock. Such a large aperture time results in high-frequency sampling errors and causes an averaging effect in the time domain.

Normally. there are some harmonics and mixing products of the input signal in the output spectrum. These non-linear distortions are produced by the errors of input amplifier and reference circuits. The kickback noise effect of the comparators on the reference signal and deviation of the reference signal from its nominal value during sampling are other sources of non-linear distortion.

Timing error and distortion are general errors in all high frequency A/D converters. The new subranging A/D converter can prevent some of these errors.

3.5 Practical Limitations of Some Types of Subranging A/D Converters

The subranging A/D converter has become increasingly popular in the last few years. A major reason for this popularity is digital signal processing, which demands high conversion speed and resolution. The traditional successive-approximation converter has reached its speed-resolution limit (about 1 μs for 12 bits) and cannot meet the demands of many applications. Although flash converters offer high speeds, they have many drawbacks that degrade the signal-to-noise ratio for high frequency analog inputs. The limitations in this structure are variable comparator delay, non-linear input capacitance and explicit sample-and-hold. Furthermore, the exponential dependence of power, area, and input capacitance on the number of bits limits its use to resolution below 12 bits. Meanwhile, the flash converter is an essential part of the subranging-A/D converter architecture [5], [7].

There are three types of subranging A/D converter architectures: conventional, pipelined, and intermeshed; each type best suits certain applications. All subranging A/D converters consist of sample-and-hold (S/H) circuits, a D/A converter, a scaling network, and timing and digital correction logic [6].

3.5.1 Conventional Subranging Converters

The conventional subranging architecture is a 2-step A/D converter, as shown in Figure 3.1. In the first step, the circuit is in the hold mode and the flash converter quantizes the input signal. After a proper scaling, the D/A converter converts the digitized and latched signal into an equivalent voltage. This voltage is subtracted from the original input

signal, yielding the difference between the first conversion and the input signal. In the second step, the difference signal is fed back to the flash converter, which amplifies and digitizes the signal. After latching, the result of this conversion goes through the digital-correction logic to produce the output. The main advantage of this subranging is that the power and area are proportional to $2^{N/2}$ for an N-bit converter, rather than to 2^N as in a flash architecture. Although a conventional subranging converter can operate half as fast as a full flash converter, there are some limitations to its speed. The delay between the first and second stage requires the use of an explicit S/H. An explicit S/H requires a high-gain operational amplifier in order to ensure a good linearity. Therefore, there are trade-offs between its gain, output voltage swing, and transient response. The D/A converter that is used in the second stage contributes delay to the path. The subtracter is usually used in closed-loop which in turn contributes a significant delay to the path. These requirements can therefore reduce the conversion rate.

3.5.2 Pipelined Subranging Converters

The second type of subranging converter has a pipelined architecture. Figure 3.2 shows this architecture. Compared with the other subranging A/D converters, the pipelined architecture offers a faster throughput rate because the circuit can initiate a new conversion before the previous conversion is finished. However, the conversion time is not significantly improved, and the digital output data corresponding to the present conversion is always delayed by at least one clock [2], [4].

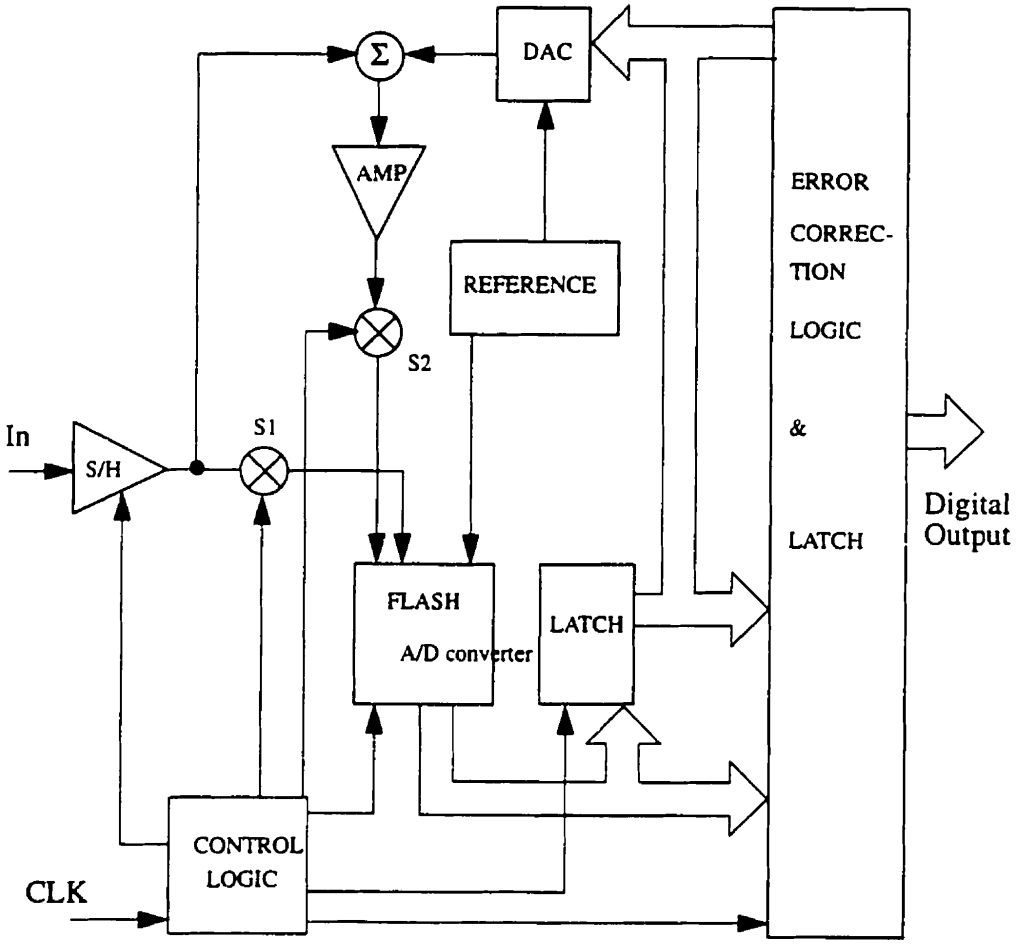

Figure 3.1 Architecture of conventional subranging A/D converter

The 2-stage pipelined converter has an extra S/H circuit and an extra flash converter. In operation, the first S/H circuit switches to the hold mode after acquiring the input signal. The first flash converter then quantizes the input signal, while the second S/H circuit goes to the hold mode. The D/A converter latches and converts the digitized signal into an equivalent voltage. This voltage is then subtracted from the held output voltage of the second S/H circuit, which represents the input voltage of the time the first flash converter made its conversion. The second flash converter amplifies and digitizes the difference

between the first conversion and the input voltage. After latching, the result of this conversion goes through the digital correction logic to produce the output. Immediately after the second S/H circuit switches to the hold mode, the input S/H can acquire the new signal, effectively increasing the throughput rate [3], [9]. While the operation of a pipelined subranging makes it attractive for high speeds, its performance relies heavily on the operational amplifier. Designing an op-amp with high gain and large output swing without any degradation in slew rate and phase margin is a challenging problem [3].

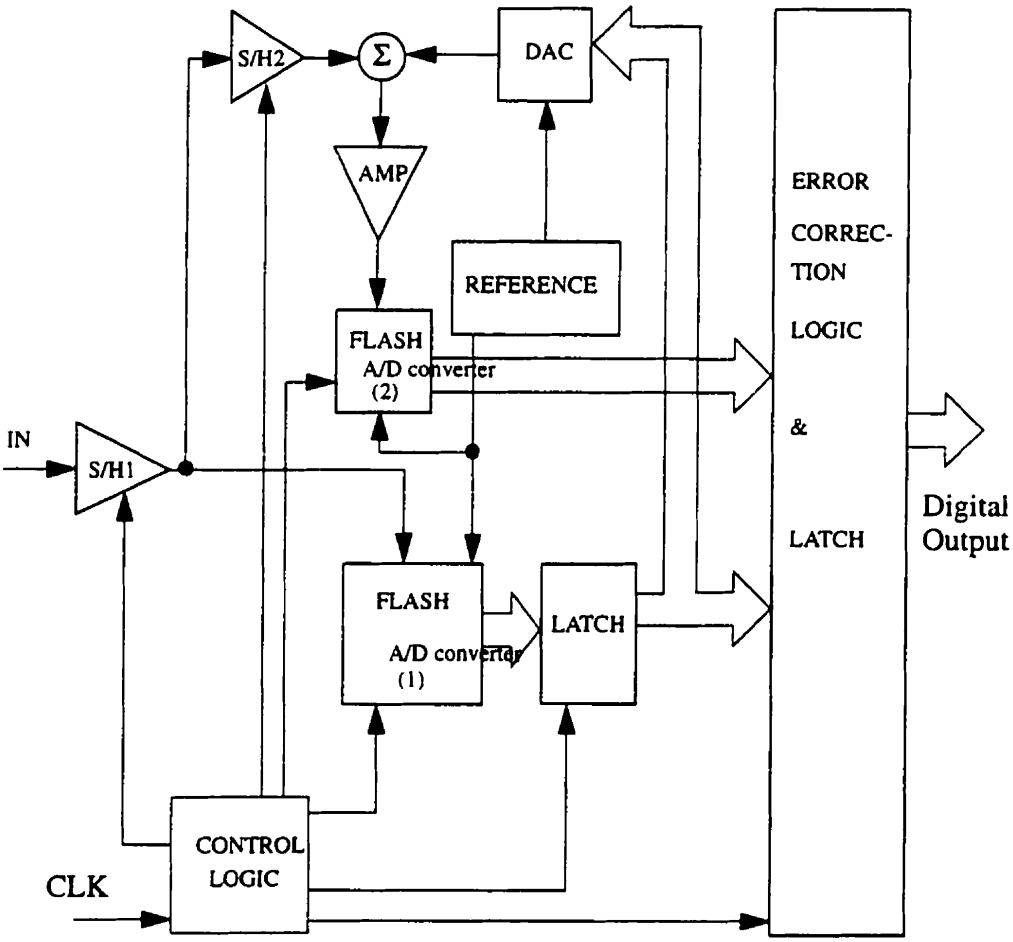

Figure 3.2 Architecture of pipelined subranging A/D converter.

3.5.3 Intermeshed Subranging Converters

Figure 3.3 shows the third type of subranging converter which uses an intermeshed architecture. This architecture eliminates the need for an explicit subtracter. After the S/H circuit acquires the signal, the first stage identifies and subdivides a reference voltage around the input voltage, and the second stage compares the input against this new set of references [7].

While avoiding the difficulties associated with subtracter designs, the intermeshed subranging architecture has some limitations. First, the reference voltage is realized with resistor ladders which generally have a long settling time. The S/H needed in this architecture must have a linearity and voltage swing compatible with the whole system which in turn limit the conversion rate. Third, the comparators in the second stage should operate across the full common-mode range of the input signal while maintaining a constant, small offset voltage.

3.6 Architecture and Algorithm of New A/D Converter

As a solution to the resolution problem in high speed conversion, an analog preprocessing circuit is proposed in this paper. Figure 3.4 shows the algorithm of the proposed A/D converter. As shown in this figure, the input analog signal will be compared with and subtracted from the different reference signals simultaneously. Therefore, the outputs of the comparator stage determine the MSBs of the converter. Meanwhile, one of the subtracter outputs will be selected by the decision center. This signal will be used by a flash stage to determine the LSBs of the converter.

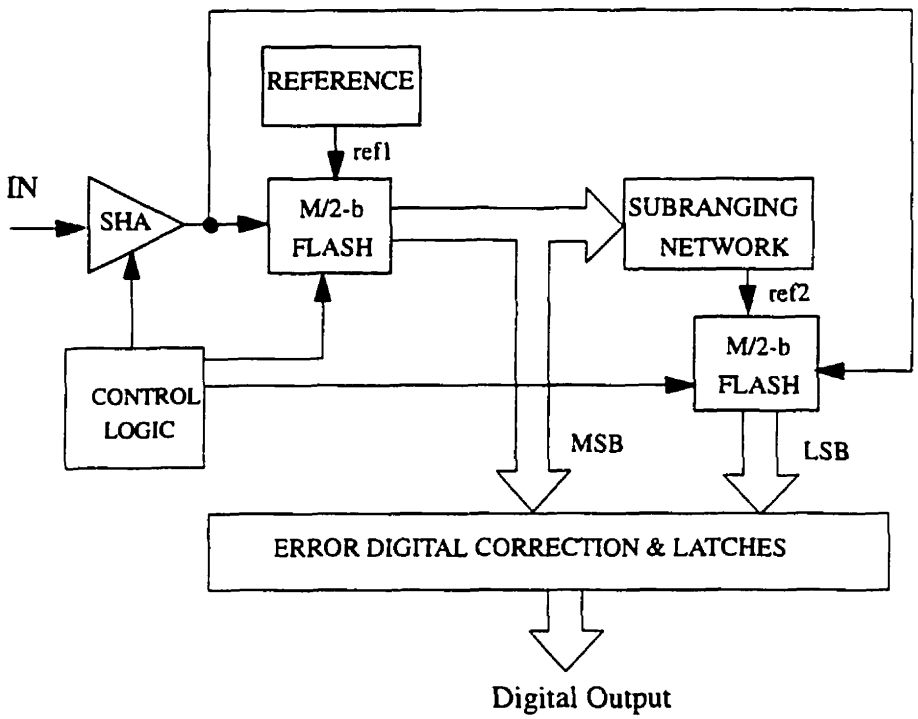

Figure 3.3 Architecture of the intermeshed subranging A/D converter.

Figure 3.5 shows the complete architecture of the proposed subranging A/D converter. This circuit consists of two main units: an *m*-bit analog preprocessing subranging circuit and a fine flash A/D converter. The other unit in Figure 3.5 is for digital error correction.

The analog subranging circuit is the fundamental unit in this architecture which consists of a comparator array, a subtracter array, a switch array, and an *m*-bit encoder, shown in Figure 3.6. The input of the subranging circuit is an analog signal and the outputs are analog and digital. The digital outputs will be encoded in order to have the *m* most significant bits by which the resolution is enhanced. The analog output is either converted by

another subranging cell or by a low resolution high speed flash A/D converter. This archi-

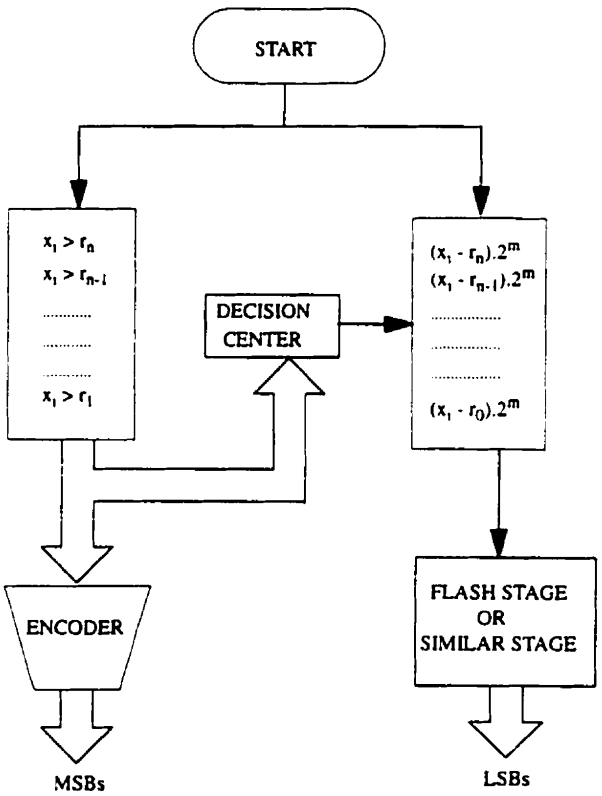

Figure 3.4 Flow chart of the subranging A/D converter.

tecture is similar to the intermeshed subranging converter except that we do not have to switch from a high reference voltage to a low one. Instead, a flash subtracter array is used to locate the range of the analog signal.

The main role of the proposed analog subranging circuit is to locate the range of an analog input signal employing an array of comparators and subtracters. The array of suborders works as a flash subtracter that gives the difference between the signal and all reference voltages. This difference is amplified by 2^m. The results of the comparator array are utilized to decode the range of the analog signal and propagate it to the output by a switch

array. The propagation delay of the analog signal in this architecture is determined by the maximum delay of the subtracters or the comparators. The delay of the switch array should also be added to that propagation delay.

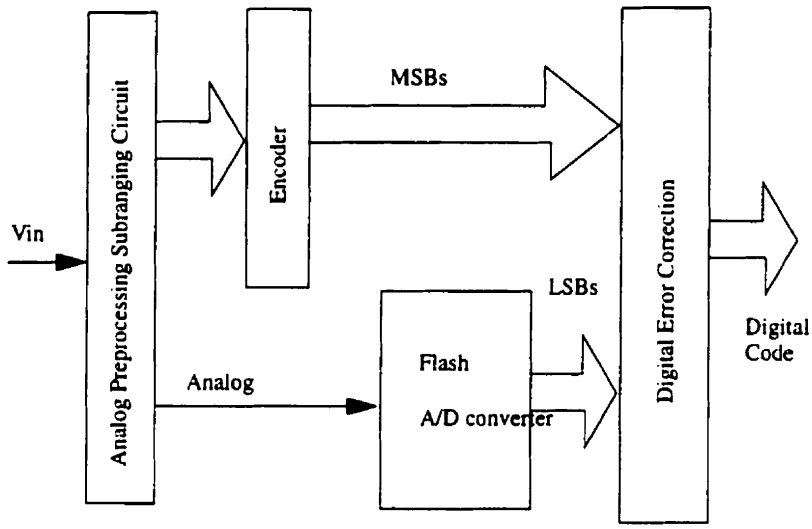

Figure 3.5 Schematic of the proposed subranging A/D converter.

3.7 Circuit Description

The performance of the proposed architecture is determined by the subranging cell's performance, Figure 3.6. The main performances that we are looking for are integral non-linearity (INL), differential nonlinearity (DNL), and the signal to noise ratio (SNR) of the system. The main sources of error are the subtracter and the reference voltage. In fact, the comparator error can be ignored whenever it does not have an effect on the digital code of

the first stage(Figure 3.4). At the same time, the effect of subtracter error on the whole A/D converter should be minimized

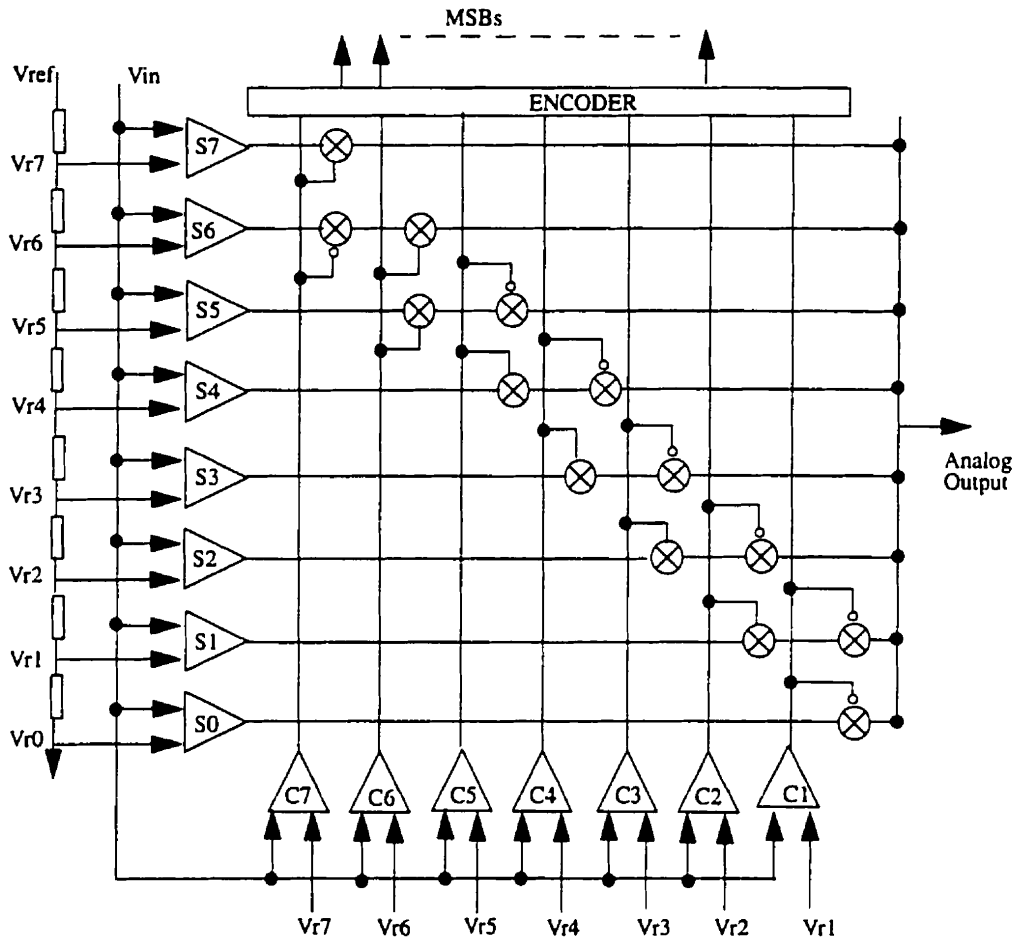

Figure 3.6 Schematic of the analog proprocessing subranging circuit used in Figure 3.5.

In the following section the designs of the subcircuits are presented. The sources of errors and their effects on the analog subranging cell performance are described.

3.7.1 Subtracter Circuit

The design of the subtracter plays a crucial role in overall system performance. The input offset voltage, delay, gain error, and output voltage swing directly influence the resolution and speed of the converter. In order to have a good integral nonlinearity, the input offset voltage should be less than 0.5 mV in an 11-bit A/D converter with a 1-V reference voltage.

Figure 3.7 shows a subtracter which employes an operation amplifier. The transient response of the subtracter depends on the performance of the op-amp used in its implementation. Since the subtracter output is no longer than 2^{N-m} LSB, where *m* is the resolution of the first stage (in this design, 256 LSB or 125 mV for N=11), the op-amp linearity, gain, slew rate, and output swing requirements are crucial in designing the A/D converter

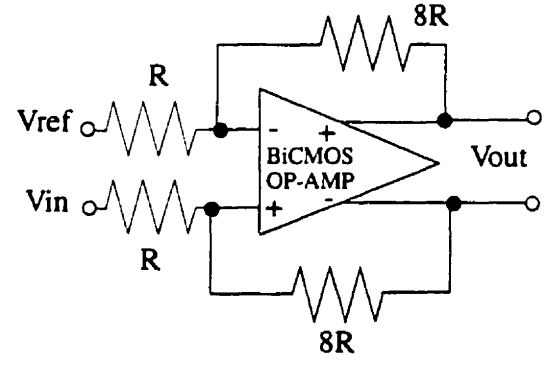

Figure 3.7 Schematic of subtracter.

Figure 3.8 shows the complete schematic of the operational amplifier employed in the subtracter[16]. The full descriptions of this amplifier has been explined in Appendix. Transistors Q1-Q2, M3-M6, and Q7-Q8 form a folded-cascade amplifier, combined with a common-mode feedback network(CMFC), M11-M14. The CMFC senses the change in the common mode output level and creates a a proportional voltage which will be feed-

back to M9 and M10 to change the bias current and hence the output's common mode volTage. Transistors M15 and M24 generate the required bias voltages.

This operational amplifier has been designed in 0.8 μm BiCMOS technology. The input transistors are bipolar because of their high transconductance, low offset voltage, low noise level. In other words, bipolar input transistors can generate less errors and higher gain with less area and DC current compared with MOS transistors. The interstage transistors are MOS transistors because of their low power dissipation and small area. In order to improve GBW and settling time, Q7 and Q8 has been implemented with bipolar transistors. In addition, the combination of bipolar and MOS transistors provide enough voltage swing in the output.

The conventional feedforward technique is used to overcome the limit of gain bandwidth(GBW) [10], [11]. The GBW in this op-amp is given by

$$GBW_{max} = \frac{f_2}{2} \tag{3.4}$$

where f_2 is the second pole of the op-amp

$$f_2 = \frac{1}{2\pi} \frac{g_{m8}}{C_{gs10} + C_{db10} + C_{eb8} + C_{\pi 8} + C_{\mu 1} + C_{cb1}} \tag{3.5}$$

which mainly depends on g_{m8} and $C_{\pi 8}$. Now, this term can be maximized by *Q8* parameters, without affecting other parameters. It is also clear that g_{m8} in bipolar technology is much bigger than in CMOS. Thus, f_2 is also increased. In this design, the second pole without feedforward compensation is 300 MHz. After feedforward compensation, it increases to 1.7 GHz. Also, in order to have a good step response, C_f should be larger than C_1 where C_1 is the total capacitance in the collector of Q1. In this design, the settling time is increased from 40 nsec to 4 nsec for $C_f = 1\ pF$.

Figure 3.9 shows the gain and phase of this amplifier. The DC gain is about 90 dB. The GBW of the amplifier is about 900 MHz and its phase margin is about 47°. The settling time of this amplifier is 4 ns, as shown in Figure 3.9.

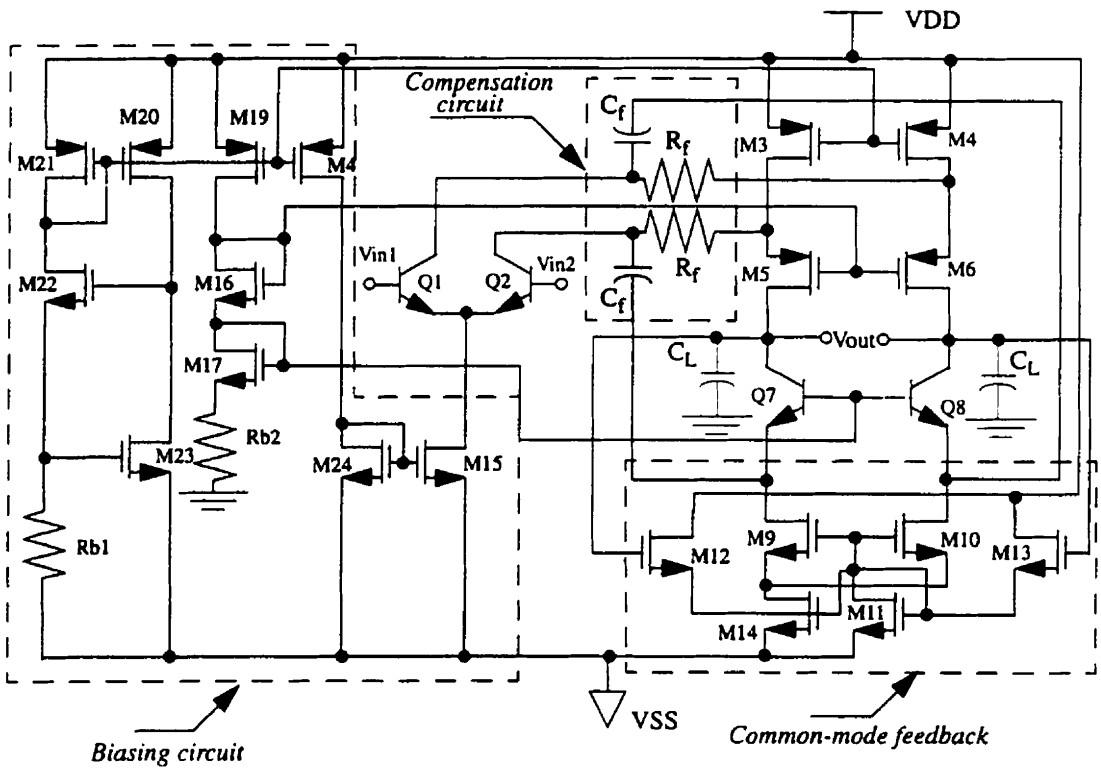

Figure 3.8 Schematic of the differential operational amplifier circuit used in the subtracter of the subranging A/D converter.

3.7.2 Comparator Circuit

Delay and offset voltage are the main parameters that affect the performance of a mixed analog circuit. The offset voltage of the comparators arrays in the analog subranging circuit has less effect than the delay of the comparator. The delay of the comparator must be less than the delay of the subtracter. Here, the design of the comparator is based on the general application, which requires low offset voltage and short delay.

To suppress linearity degradation due to comparator inaccuracy, the comparator should in general have a low offset voltage. Moreover, a CMOS comparator suffers from the large offset voltage of its latch. In contrast, BiCMOS technology has the potential for a low offset voltage. Moreover, all switches have been implemented with MOS transistors because of their zero-offset and low leakage. In the proposed subranging A/D converter, the comparison and comparator circuit techniques presented by Razavi [12], [13] are employed.

Figure 3.10 shows the architecture and timing of the BiCMOS comparator. Figure 3.11 shows the comparator circuit, which consists of a preamplifier(M1-M2 and Q1-Q4), offset storage capacitor(C1-C2), a bipolar latch(Q5-Q6 and M11-M12), and a CMOS latch (M3-M10). It is controlled by two clocks, $\phi 1$ and $\phi 2$. The circuit operates as follows. In the calibration modes, S1 and S2 are off and S3-S6 are on, thereby grounding the inputs of the preamplifiers and the bipolar latch. The preamplifier input offset is thus amplified and stored on C1 and C2. In this mode, the two latches are also reset. In the comparison mode, first S3-S6 turn off while S1 and S2 turn on; the input voltage, V_i, is sensed and amplified, generating a differential voltage at the bipolar latch input. Next, the two latches are strobed sequentially to produce +5 V at the output.

The resolution of the comparator depends on both its input offset voltage and its input-referred noise. The residual input offset of this comparator is determined by the bipolar latch offset divided by the preamplifier gain [12].

$$V_{os} = \frac{V_{oslB}}{g_{mQ}R_C} + V_{os(Q1-Q2)} + V_{osM} + \frac{KT}{q}\frac{\Delta R_1}{R_1} \tag{3.6}$$

where V_{oslB} is the offset latch of the bipolar latch and $g_{mQ}R_C$ is the gain of the preamplifier where R_C is the equivalent resistance at the collector of Q1. The offset voltage of the bipolar latch is given by

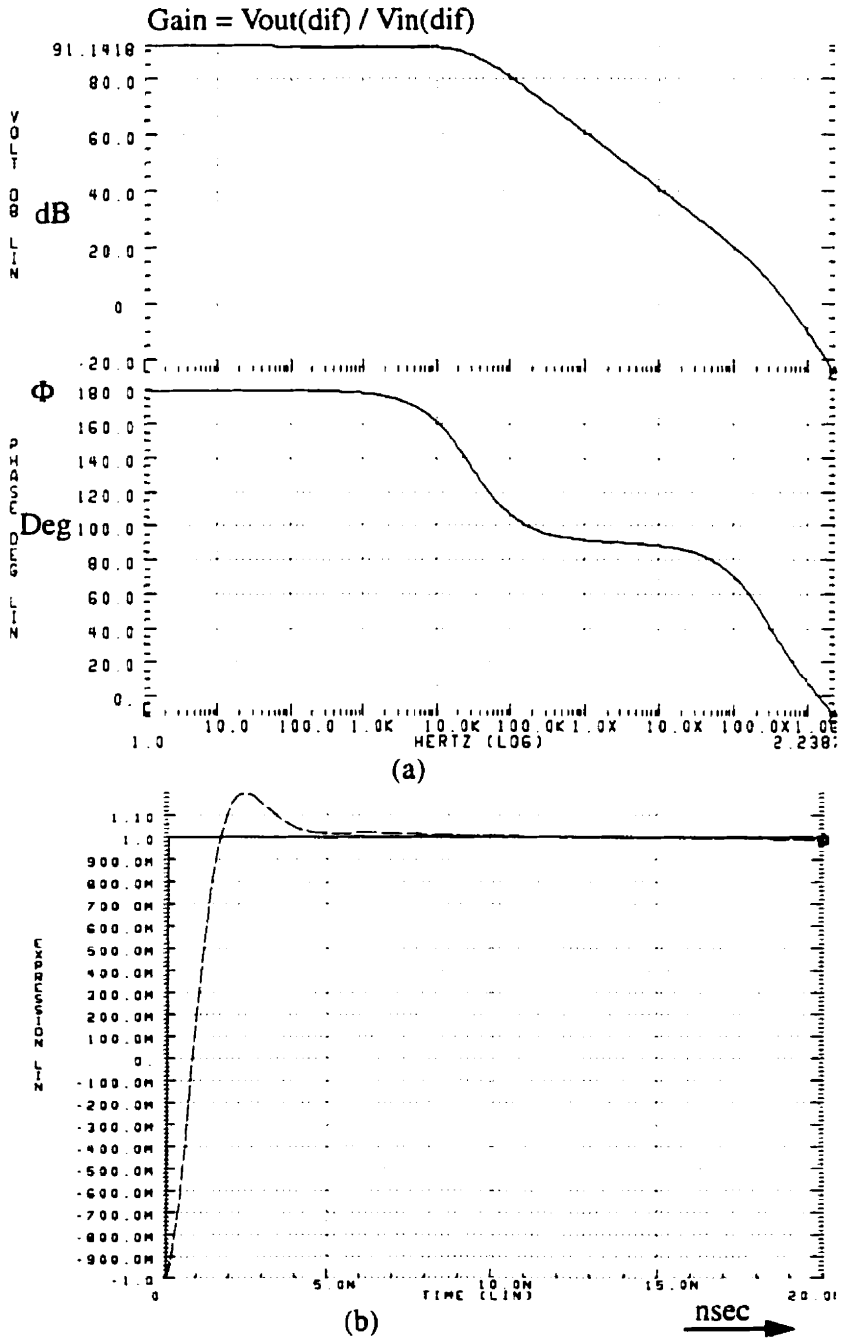

Figure 3.9 The characteristics of BiCMOS opamp: (a) Gain and Phase margin (b) Settling time

$$V_{os(Q1-Q2)} = V_{osIB} = \frac{KT}{q} Ln \frac{\Delta I_S}{I_S} \approx \frac{KT}{q} \frac{\Delta A}{A} \tag{3.7}$$

where KT/q is the thermal voltage, ΔI_S and I_S are the standard deviation and mean value of the saturation current, respectively, and ΔA and A are those of emitter areas. The offset voltage of input MOSFET pair is equal to

$$V_{osM} = \Delta V_{TH} + \frac{1}{2}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)(V_{GS} - V_{TH}) \tag{3.8}$$

where ΔV_{TH}, ΔW, and ΔL *are* the standard deviation of threshold voltage, width and length of transistors respectively.

The main source of noise in the preamplifier are shot noise and thermal noise. The input-referred noise power density of the preamplifier is given by

$$\frac{\overline{v_n^2}}{\Delta f} = 4KT\left(\frac{1}{g_{mQ}}\right) + 4KT\left(2r_b + 2R_{SW} + \frac{2}{g_{mM}}\right) \tag{3.9}$$

where g_{mQ} and r_b are the transconductance and base resistance of $Q1$ and $Q2$, R_{SW} is the on resistance of the input switches, and g_{mM} is the transconductance of $M1$ and $M2$.

To improve the dynamic range of the comparator, the input transistors($Q1$, $Q2$) must be large and wide (to reduce input offset and r_b) and the bias current of $Q1$ and $Q2$ must increase (to increase g_{mQ}). These modifications will, in turn, increase the input capacitance. Therefore, there is a trade off in this design. Here, $Q1$ and $Q2$ are implemented in a 3.2 μm emitter area. They are biased at 400 μA dc of current.

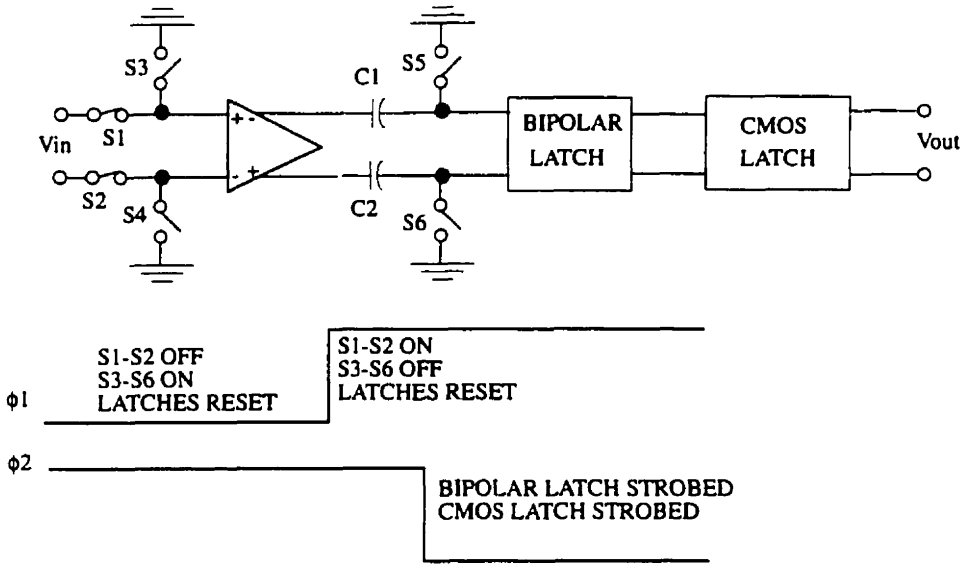

Figure 3.10 Block diagram of the comparator

In the proposed subranging A/D converter, it is preferred that the delay time of the comparator be less than the settling time of the subtracter. The delay of the comparator consists of two main delays; recovery time of the preamplifier and the regeneration time constant of the latch. The delay of the designed comparator is dominated by the recovery time of the preamplifier.

The preamplifier, followed by a source follower, isolates the latch capacitance from the gain amplifier at the expense of adding some group delay. Also, the source follower has the added benefit of buffering the gain amplifier from the kickback charge of the dynamic latch.

The step response for the single-stage amplifier plus source follower is approximated by

$$V_{la} = V_{in}g_{mQ}R_C + (V_{EE} - I_0R_1 - V_{in}g_{mQ}R_C)\exp\frac{-t}{R_CC_{tot}} \quad (3.10)$$

where V_{la} is the differential voltage of the bipolar latch, g_{mQ} is the transconductance of $Q1$, C_{tot} is the total parasitic capacitance at the collector of $Q1$ which includes the effect of C_1 (C_1/β_3), and R_C is the total resistance of the collector node of Q_1.

The recovery time is tested when the input is changed from full scale range to 1 LSB. Therefore, this change of input voltage must produce a minimum differential voltage for the latch(V_{lamin}). Hence the recovery time of the preamplifier is given by

$$t_d = R_CC_{tot}Ln\left(\frac{V_{EE} - I_0R_1 - V_{LSB}g_{mQ}R_C}{V_{lamin} - V_{LSB}g_{mQ}R_C}\right) \quad (3.11)$$

The bipolar latch must behave so that it can generate a high voltage from a very low differential voltage in a short time. This will be performed by positive feedback around Q5 and *Q6*. Capacitor C_3 discharge to V_{EE} during calibration and the latch is off. When $\phi 1$ is high, the latch starts its operation by passing current through M12 and C_3. This will continue until the steady state of the bipolar latch is reached.

The CMOS latch is off during calibration and M9 and M10 switch nodes X2 and Y2 to V_{EE}. The offset voltage of the CMOS latch cannot allow it to operate simultaneously with the bipolar latch. Therefore, there is a delay between the starting time of the CMOS latch and the bipolar latch. This delay is controlled by C_3 and G_1.

Figure 3.12 shows the simulated waveforms of the comparator to ramp input. After the analog input is sensed (*40nsec*) the bipolar latch is strobed and a 10 nsec later the CMOS latch is activated. Therefore, the comparator rate is 20 MHz.

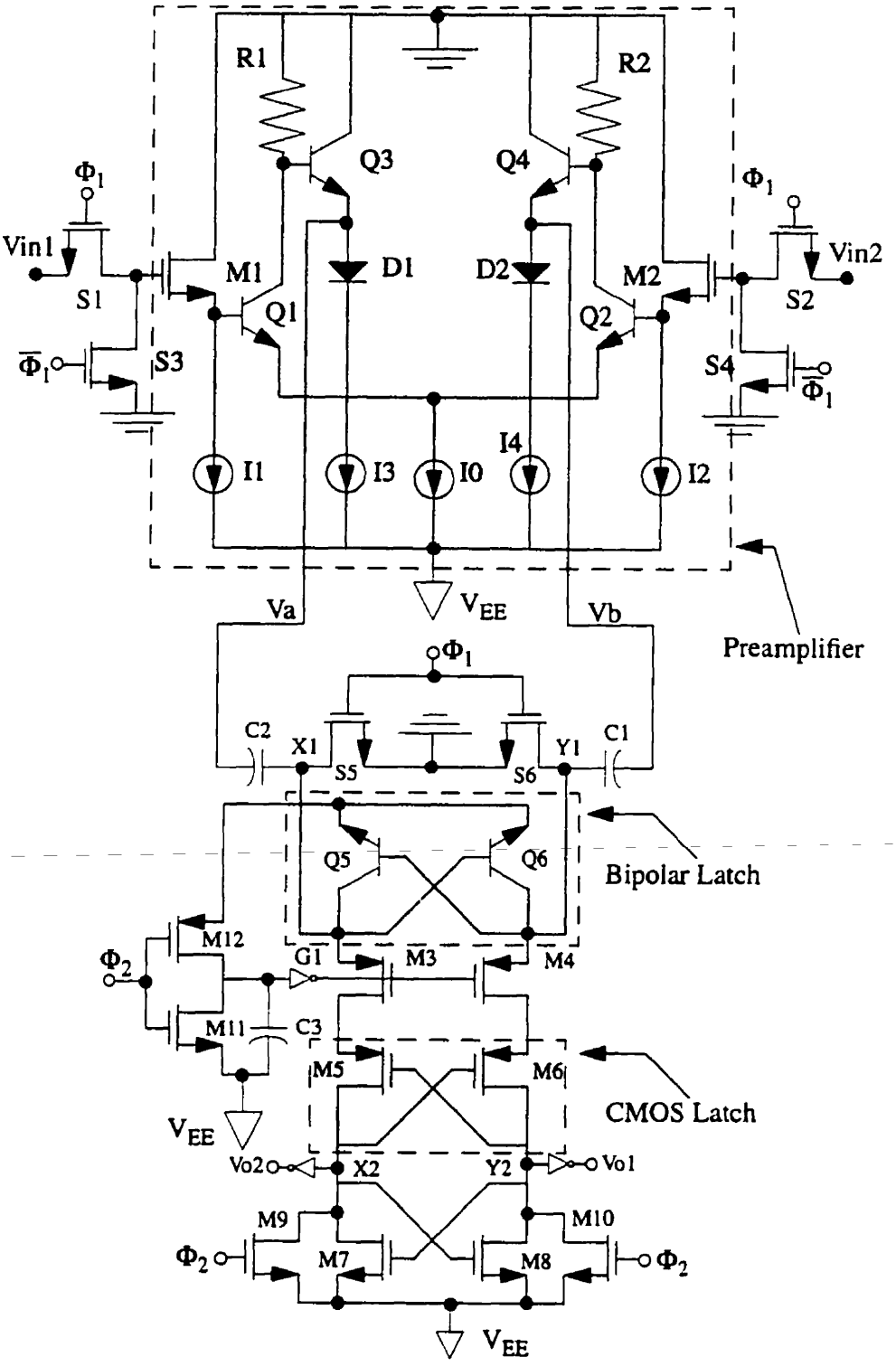

Figure 3.11 Schematic of voltage mode comparator.

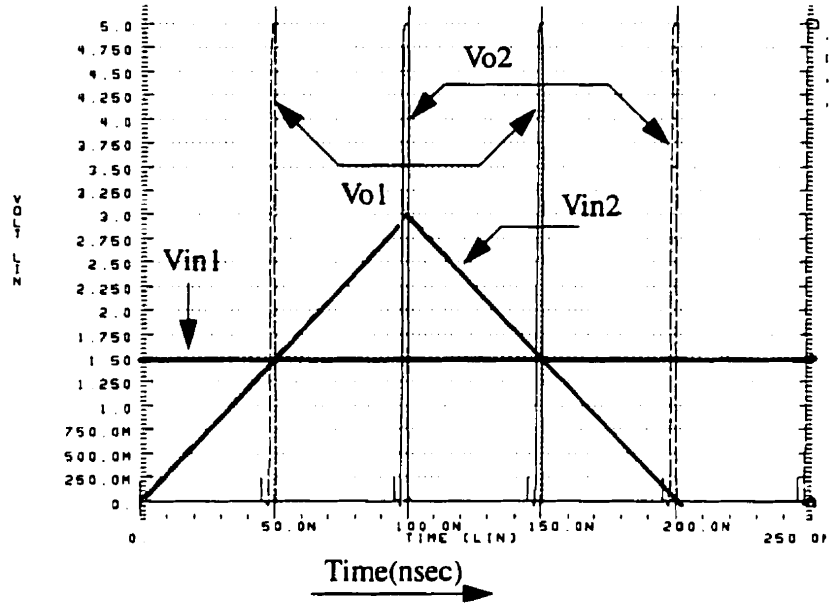

Figure 3.12 The simulation results of the comparator with ramp input.

3.7.3 Voltage Reference

The reference voltages for the first part are generated using resistor ladders, as shown in Figure 3.13. An important aspect of resistor ladders is the differential and integral non-linearity errors. These errors result from mismatches in the resistors comprised the ladder. Based on the Gaussian probability density function for the value of each resistor, the standard deviation of the tap voltage of a resistor ladder with a mean equal to $j\ V_{REF}/N$ is[14]

$$INL_J = \sqrt{\frac{J}{N^2}\left(1-\frac{J}{N}\right)}\frac{\Delta R}{R}V_{REF} \tag{3.12}$$

The maximum of this error at $J = N/2$ is equal to

$$INL_{max} = \frac{1}{\sqrt{4N}}\frac{\Delta R}{R}V_{REF} \tag{3.13}$$

Eq. 3.13 shows that *INL* can be reduced by increasing the resolution. Therefore, the reference error of the first stage in the proposed subranging A/D converter will introduce an error to the second stage. For example, if a 3-bit stage is followed by an ideal 8-bit flash converter with V_{REF} of 1*V*, and INL_{max} < 1/2 LSB, it is required that $\Delta R / R$ be less than 0.15%.

The speed of the converter can be affected by the equivalent resistance seen at each tap. This resistance, with the input capacitance of the comparator and the subtracter, reduce the speed of conversion. This resistance will reach to a maximum of *NR / 4* at the midpoint.

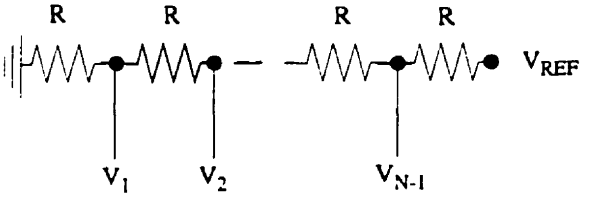

Figure 3.13 Resistor ladders for the reference voltage.

3.7.4 Switched Logic

One of the subtracter outputs must be selected for the next stage. This will be done by a switching unit. This unit can be implemented by a CMOS switch, as shown in Figure 3.6, or by a CMOS logic gate, shown in Figure 3.14. The delay of this switching control unit must be lower than the delay of the subtracter. In other words, the total delay of a comparator plus the switching control unit must be equal to the delay of the subtracter.

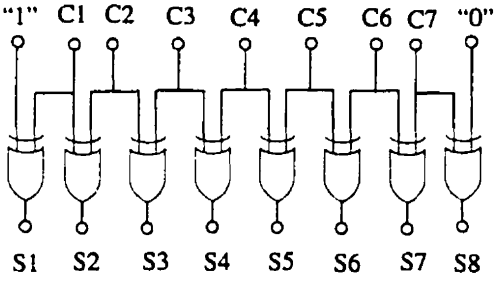

Figure 3.14 Logic unit for the interface between the comparator array and the subtracter array.

3.8 A/D Converter Implementation

In order to verify the performance of the proposed subranging A/D converter, subcircuits have been fabricated using 0.8 μm, double-poly, double-metal BiCMOS technology. The threshold voltages are 0.8 V for NMOS and -0.85 V for PMOS. The f_T of the bipolar transistor is 11 GHz. In order to reduce parasitic elements and gate resistance, the transistors are integrated with an inter-digit layout. Fig. 14 shows the prototype die photo of subcircuits used in a subranging A/D converter.

The areas of the comparator and subtracter are about 0.06 mm^2 and 0.09 mm^2. In order to reduce area and to increase the accuracy, the resistor ladder for the reference voltage is realized with polysilicon. The nominal value of the resistor is 750 Ω/sq. The resistors in the ladder are1 $k\Omega$, which in turn occupy the 5.6 μm^2 area.

3.9 Experimental Results

In order to verify the proposed A/D architecture, the subcircuits have been fabricated and tested. First, the designed op-amp has been tested. Table 3.1 shows some of the experimental results of the BiCMOS op-amp. The experimental results shows a satisfactory agreement with simulation results.

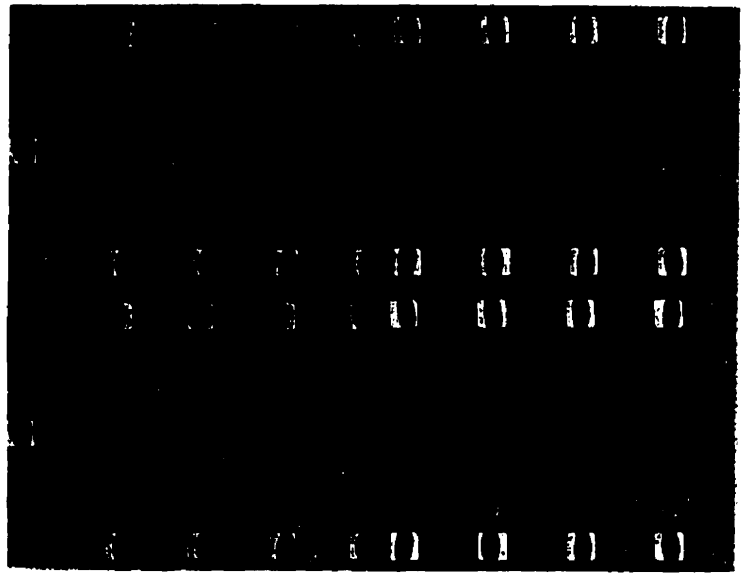

Figure 3.15 Prototype die photo of the subcircuits used in the subranging A/D converter

Table 3.1 The characteristic of the BiCMOS amplifier

Parameters	Simulation	Experimental
VDD, VSS	+/- 2.5V	+/-2.5
power dissipation	25 mW	50 mW
DC gain	90 dB	>65 dB
GBW	900 MHz	>100 MHz
Phase margin	47°	~50
Input Offset Voltage	< 20 μV	100-500 μV
Single output swing	+/- 1.5	+/- 1.1 V
Single slew rate	100 V/μS	80 V/μS
Load capacitance	2 pF	2 pF

Table 3.2 shows the experimental results of the comparator test. The offset voltage and power dissipation are greater than those in the simulation results.

Table 3.2 The comparator performance

Parameter	Simulation	Experimental
Input Offset Voltage	200 μV	1 mV
Comparator Rate	20 MHz	> 2 MHz
Input Range	3 V	
Power	5 mW	10-15 mW
Power Supply	+5 V	+5 V
Area	0.06 mm^2	0.06 mm^2
Technology	0.8 μm BiCMOS	0.8 μm BiCMOS

Therefore, both experimental results gave us enough information to design a setup for testing the proposed A/D converter.

3.10 System Performances of A/D Converter and Its Test

In order to show the performance of the proposed subranging circuit in speed and resolution enhancement, the subranging cell is used as a resolution enhancement of three bits to an 8-bit flash converter. Therefore, a 3-bit subranging cell was designed, fabricated and tested. Then, this subranging cell was used with an 8-bit flash A/D converter to arrive at an 11-bit A/D converter.

3.10.1 System Analysis

In order to analyze the proposed A/D converter, it is required to have a useful analysis tool. The FFT is a general tool which converts the A/D converter output from the time domain to the frequency domain. The FFT output spectrum contains the input sine wave test signal, a noise floor caused by quantization errors, and harmonic distortion caused by *INL* and *DNL* errors. The most fundamental performances which are traditionally tested by FFT are signal-to-noise ratio(*SNR*), signal-to-noise-without distortion ratio (*SNWR*)

and the effective number of bits (*ENOB*). In addition, total harmonic distortion(*THD*) measures the quality of the transmission of a tone.

Parserval's relation for the FFT states that

$$\sum_{n=0}^{N-1} |x(n)|^2 = \frac{1}{N} \sum_{k=0}^{N-1} |X(k)|^2 \tag{3.14}$$

where *x(n)* is an *N*-point time sequence and *X(k)* is the result of an *N*-point FFT being applied to x(n). The computation of the *THD* is accomplished by a ratio of signal power to noise power. Assuming that the desired signal is a single frequency component in the *j-th* element of the FFT output vector *X*, then:

$$THD = 10\log \frac{X(j)^2}{\sum_{k=0}^{\frac{N-1}{2}} |X(k)|^2, k \neq j} \tag{3.15}$$

The *SNWR* is deduced from the quantification step. The quantification step (*Q*) is deduced from the quantization error (*QE*) which is the *RMS* of the quantization noise.

$$QE_{rms} = \frac{Q}{\sqrt{12}} \tag{3.16}$$

$$SNWR = 20\log \frac{1}{Q} \tag{3.17}$$

The *SNR* is combination of the *THD* and *SNWR* ((3.18)).

$$SNR = -20\log \sqrt{10^{-\left(\frac{SNWR}{10}\right)} + 10^{-\left(\frac{THD}{10}\right)}} \tag{3.18}$$

The *ENOB* is directly deduced from the *SNR*. In fact, the *SNR* is given by $SNR = 6.02n + 1.76dB$, and consequently the *ENOB* is given by the following equation:

$$ENOB = \frac{SNR - 1.76dB}{6.02} \tag{3.19}$$

3.10.2 A/D Converter Test

The main characteristic that we are looking for in this architecture is an increase in the resolution of a flash A/D converter without degrading the speed. Thus, the subranging cell should give an output voltage which has the precision of the whole conversion system (11-bit). As mentioned earlier the main source of error is the subtracter array. With the proposed subtracter design, the eleven bit resolution can be guaranteed, for this example. Also, we have proved that the speed of the subranging cell is determined by the settling time of the subtracter. Thus, the subranging circuit can follow the speed of the flash converter.

In this application, an 11-bit subranging A/D is considered. In order to arrive at an 11-bit A/D converter an 8-bit commercial flash A/D converter is used with a 3-bit subranging cell designed and implemented as described. The three most significant bits are extracted using the subranging cell and the difference between the remaining of the signal is converted using the flash converter. Figure 3.16 shows the setup for the test of proposed A/D converter.

Meanwhile, the performances of this 11-bit subranging converter are tested on two cases; nominal and faulty. The nominal test is based on the experimental results and the test setup in Figure 3.16. The faulty test is based on the HSPICE simulation results,

including worst-case errors in the testing of the BiCMOS op-amp and comparator. Table 3.3 shows the test condition in nominal and faulty conditions.

The performances studied are: *INL*, *DNL*, total harmonic distortion (*THD*), signal to noise ratio without distortion (*SNWR*), signal to noise ratio plus distortion (*SNR*) and effective number of bits (*ENOB*).

Table 3.3 Nominal and faulty test condition

Parameter	**Nominal**	**Faulty**
Subtracter Offset voltage	+/- 0.6 mV	2.5 mV
Variation of Offset Voltage	-0 %	-20%-->300%
Gain error variation	0.01 %	+/- 0.25 %
Resistor ladder variation	0 %	+/- 2 %

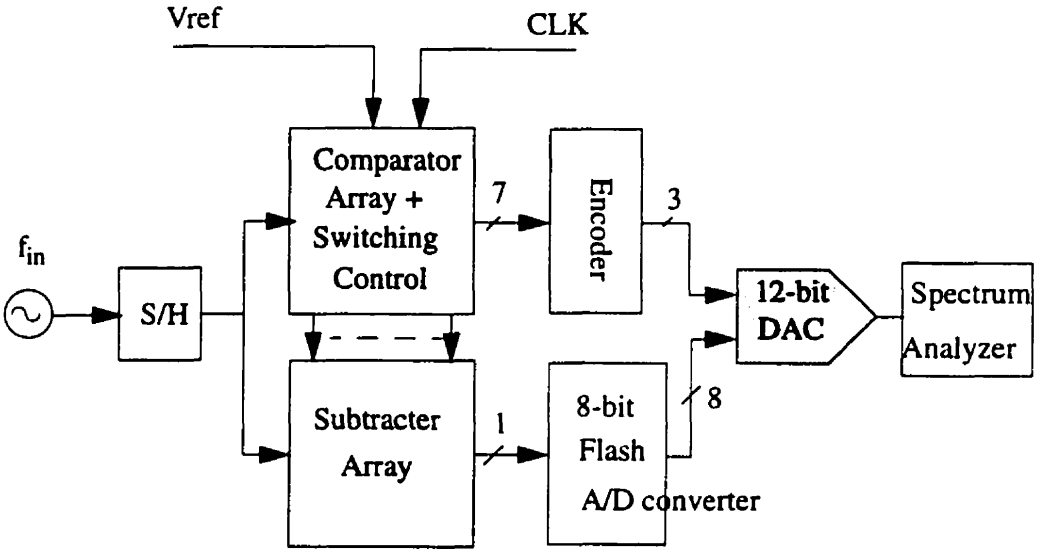

Figure 3.16 Test setup for testing of the 11-bit subranging A/D converter.

Based on the setup test of Figure 3.16, the 3-bit subranging cell was tested followed by an 8-bit commercial flash A/D converter. The experimental data and FFT tool were used to calculate the errors in A/D converter. Since we are using eight subtracters, different performances are considered for each subtracter. Thus, each subtracter has its own gain error, offset, and linearity. The nominal offset of the subtracters is between *-0.6 mV* and *+0.6 mV*. The maximum linearity variation is 0.01% and the gain error is 0.01%. Using this realistic error we found that the quantification step $Q = 5.055 \times 10^{-4}$ V which gives a *SNWR=65.9dB* ((3.17)), and the total harmonic distortion is *THD=64.3dB*. This gives a signal to noise ratio, *SNR=62dB* ((3.18)). From the quantification step we found the resolution of the A/D which is *10.95* bits. The effective number of bits is deduced from the *SNR* using (3.19) and this gives *ENOB=10.3* bits.

Figure 3.19 shows the *INL* and *DNL* error of the 11-bit A/D converter in the nominal cases. Figure 3.18 illustrates the spectrum of the quantified signal in nominal cases. It can be seen that the frequency of the quantified signal is 1MHz.

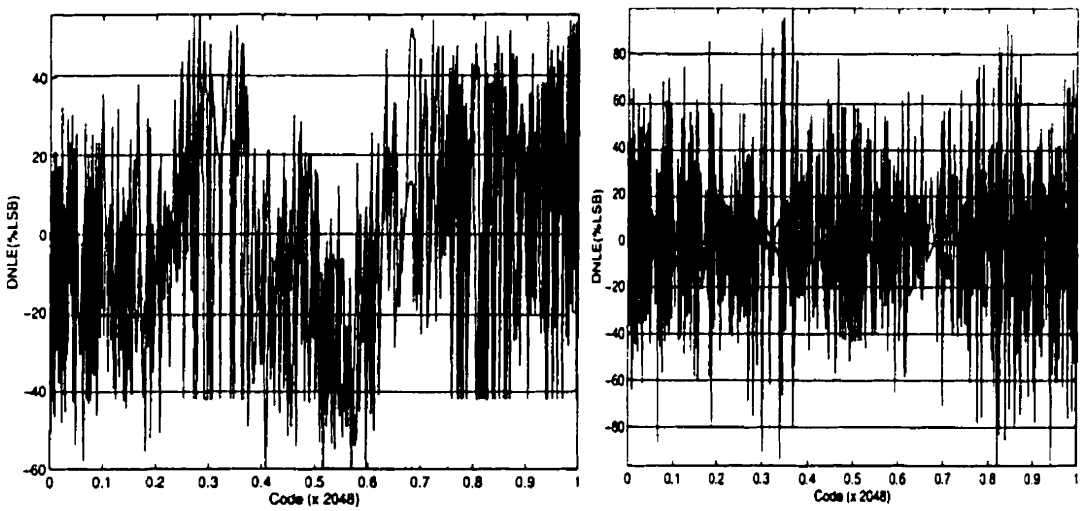

Figure 3.17 INL and DNL error in nominal conditions

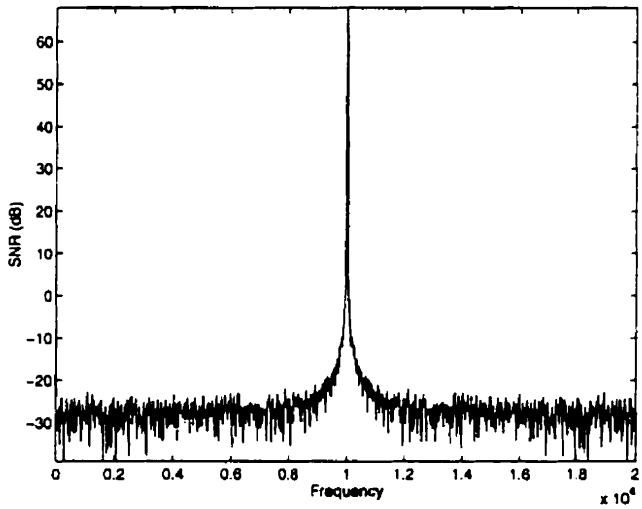

Figure 3.18 Spectrum of the quantified signal in nominal cases for fin = 1 MHz

In the faulty case, the worst case experimental results of subtracter and comparator are included in the test of the A/D converter. Then, the effect of these errors on the performances of the A/D converter are analyzed by employing HSPICE and MATLAB simulator. Figure 3.19 shows the *INL* and *DNL* error in faulty test. It seems that the gain and offset error increase the *INL* and *DNL* to 200% of LSB in some codes. It also shows some missing codes(i.e. code 1032 LSB). Figure 3.20 illustrates that the *THD* and quantification noise power are about 60 dB and 56.3 dB, respectively. The *SNR* of A/D converter is about 55 dB which gives 9.13 bit as *ENB*. Table 3.4 summarize the test results in nominal and faulty conditions.

Table 3.4 Nominal and faulty test results

Parameters	Nominal	Faulty
SNWR	66 dB	61 dB
Effective bit: fin = 1MHz	10.3 bit	9.13 bit
SNR	62 dB	55 dB
THD	64.3 dB	60 dB
INLE	0.6 LSB	2 LSB
DNLE	0.8 LSB	2.5 LSB

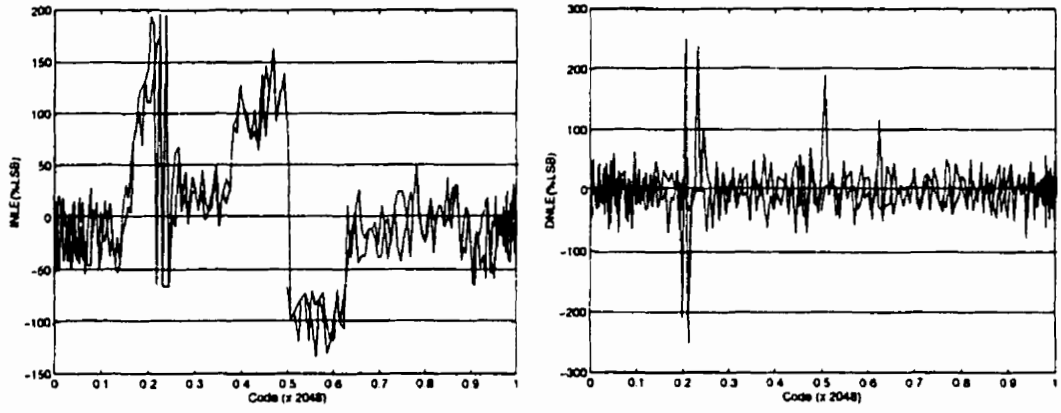

Figure 3.19 INL and DNL error test result in subranging A/D converter

3.11 Summary and Conclusion

A novel architecture for a subranging A/D converter which performs the subtraction and comparison simultaneously is proposed and applied to an 11-bit video-rate A/D converter. A operational amplifier with a 4-ns settling time, a 90-dB dc open-loop gain, and 900 MHz unity-gain is employed in the subtracter. A high performance comparator with 100 μV offset voltage has been designed to perform the comparison for a 20 MHz analog signal. The subcircuits are realized with 0.8 μm BiCMOS technology.

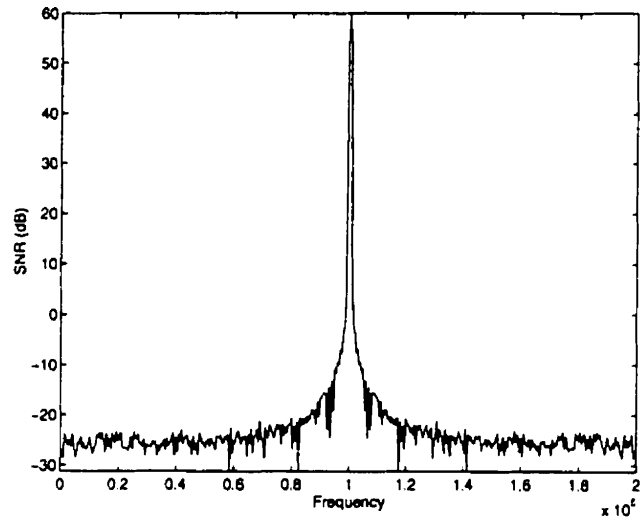

Figure 3.20 Spectrum of the quantified signal for fin = 1 MHz

This A/D converter consists of a 3-bit subranging cell and an 8-bit conventional flash A/D converter. The speed of conversion has been improved by flash subtracters and eliminating the S/H in the input. The second stage of the converter employed a fine flash converter. We have demonstrated that this A/D converter has the potential to have a 11-bit resolution at 1 MHz. The SNR in the nominal case is 62-dB, which shows that 10-bit as effective number of bits.

3.12 References

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CHAPITRE IV

Un commutateur actif en mode courant pour des applications de hautes performances à faibles tensions

4.1 Résumé

Dans le chapitre précédent, l'architecture du convertisseur A/N proposée a été validée en mode tension. Cependant, la capacité du mode courant nous a encouragé à explorer cette architecture en mode courant; et ceci constitue l'objectif de ce chapitre et du chapitre 5.

Ce chapitre présente un nouveau regard sur les cellules de mémoire comme interrupteur en mode courant. Les cellules de mémoire en mode courant sont caractérisées par des paramètres de commutation comme la perte d'insertion, l'isolation, et la bande passante. Ce regard nous aide à analyser quelques circuits opérant en mode courant en se basant sur les performances de commutation.Suite à cette analyse, un interrupteur à faible insertion et à faible courant actif est conçu, fabriqué et testé.

L'architecture de l'interrupteur proposée est basée sur la régénération du signal plutôt que sur sa propagation, comme dans les interrupteurs de tension conventionnel. Cette technique de commutation du signal appliquée aux amplificateurs et aux mécanismes d'ajustement permet de réduire la sensibilité du système à la résistance en conduction de l'interrupteur.

L'interrupteur en mode courant proposé qui est utilisé dans la matrice contient un circuit d'écriture de courant, des interrupteurs, un lecteur de courant et un circuit de logique de contrôle. Le circuit d'écriture de courant détecte et enregistre le courant d'entrée. La logique de contrôle permet au lecteur de courant de lire le courant d'entrée de l'écréteur de courant. Les sources de courant de référence du circuit font en sorte que le courant de sortie soit proportionnel à celui de l'entrée.

L'interrupteur en mode courant a été conçu et implanté avec la technologie CMOS 1.2 µm de MITEL. Les résultats expérimentaux sont satisfaisants. Le perte d'insertion et l'isolation sont 0.56 dB et 60 dB respectivement. La surface de l'interrupteur est de 0.02 mm^2 avec une alimentation de 3V.

L'interrupteur proposé peut être utilisé dans tous les circuits en mode courant comme les systèmes de commutation, les CAN mode courant. Les contributions principales de l'interrupteur proposé sont qu'il peut supporter le passage du signal dans une direction, une faible perte d'insertion, une isolation élevée et une faible consommation de puissance. D'autres contributions sont sa grande vitesse et sa faible surface qui permettent une intégration à grande échelle.

Dans la première partie, l'architecture de l'interrupteur mode courant est décrite. L'interrupteur proposé est ensuite analysé et comparé avec l'interrupteur en mode tension. Les différentes applications sont aussi expliquées. Les résultats expérimentaux avec les résultats de simulation font l'objet de la dernière partie. Notons que l'article proposé dans ce chapitre a été soumis au "IEEE Journal of Solid-State Circuits".

Active Current Mode Switch for High Performance and Low Voltage Applications

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Note: This paper has been submitted for publication to the IEEE Journal Solid-State Circuits.

4.2 Abstract

This paper presents a new view of current memory cell as current mode switch. The current momery cell is characterized with switch parameters such as insertion loss, isolation, and bandwidth. This view helps us to analyze some of the current mode design based on switching performance. Based on this analysis, a low insertion loss active current switch is designed, fabricated and tested.

The proposed switch architecture is based on signal regeneration rather than on signal propagation which is used the conventional voltage mode switch. This switching technique enables signal buffering and adjustment to reduce the sensitivity of the system to the "on" resistance of the switch.

The proposed current mode switch used in the array includes a current writer, switches, a current reader, and control logic circuit. The current writer detects and saves

the input current. The control logic enables the current reader to read the input current from the current writer. The circuit's reference current sources enable the output signal to be a current signal proportional to input current.

The current mode switch has been designed and implemented in CMOS $1.2\mu m$ MITEL technology. The experimental results show satisfactory results. The insertion loss and isolation of current mode switch are $0.56\ dB$ and $60\ dB$ respectively. The area of switch is $0.02\ mm^2$ with $3\ V$ power supply.

The proposed switch can be used in any current mode design like fully electrical switching system with current electrical signal as input, current mode S/H, current mode A/D converter. The main contributions of the proposed switch are that it can handle unidirectional signal transmition, low insertion loss, high isolation, and low power dissipation. High speed and small area are the other contributions which in turn enable the proposed switch for high integration level.

4.3 Introduction

One of the keys to the future of telecommunications companies will be their ability to provide new broadband services to both the business community and the residential customer. These new services include the transfer of video signals, high-definition TV, high-data-rate file transfers, information retrieval, and animated graphics, and should include the interconnect for diskless workstations and local area networks/metropolitan area networks (LANs/MANs). Such services will require a very high-performance switch array providing connectivity between input ports and output ports.

Among the most challenging specifications of the switch array are its insertion loss, isolation, power dissipation and bandwidth. These are the main limitations to have a high-

density and very fast switch matrix at a reasonable price. In order to design a high-performance switching matrix at very low cost, a novel switch array architecture is needed. Although voltage-mode switches can optimize some of these limitations, insertion loss and speed are still challenging problems which require to design the switch in another mode of operation.

Current-mode circuits are rapidly becoming a topic of wide interest[1], [2], [3], [4]. Current-mode technique(in which the signal is essentially processed in the current domain) offer a number of advantages. Generally current mode circuits do not require amplifiers with high voltage gains, thereby reducing the need for high-performance amplifiers. At the same time current-mode circuits generally do not require either resistors or capacitors, and, when capacitors are used to store the signal, they need not display either good ratio matching or good linearity. Therefore, current-mode circuits can be designed almost exclusively with transistors, making them fully compatible with most digital processes. The current-mode circuit also has a low power supply voltage requirement, since it uses wideband current mirrors as amplifiers as opposed to switched-capacitor circuits which employ voltage operational amplifiers.

The current-mode technique has proved its ability in designs of different kinds of analog circuits like analog memory, the current sampler, current mode A/D converter, and the switched current filter.

This paper will mainly be associated with the application of current-mode circuits in electrical circuits; more particularly, it pertains to an electrical switch with low insertion loss operating at high speed which is suitable for high performance application.

In the first part, the architecture of current mode switch is described. Secondly, the proposed switch is analyzed and compared with voltage mode switch. The various applications of current mode switch are explained. The experimental results with simulation results are shown in the last part.

4.4 Unidirectional Current Mode Switch

4.4.1 Architecture of Current Mode Switch

The switching matrix mainly consists of some current memory cells. The current memory cell is based on signal regeneration instead of signal transmission. Figure 4.1 shows the architecture of this unit which consists of a current write unit (CWU), a current read unit (CRU), a controlled current source (CCS), a switch (SWI), and logic control unit (CLU).

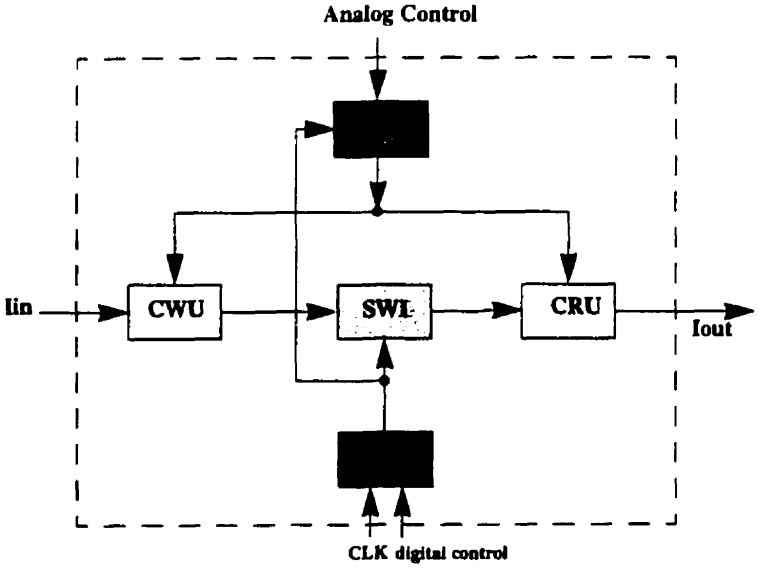


Figure 4.1 Block diagram of the current mode switch.

Speed and accuracy are two main advantages of current-mode approach. The current-mode approach relies on the use of current mirror to achieve higher performance. Different kinds of current mirror like simple current mirror, wilson current mirror, cascode current mirror have been studied and explained in textbook[64]. Each of these kinds of current mirror is suitable for special kind of application. Here, the simple current mirror is shown in Figure 4.2 . Although, it is recommended to replace simple MOS transistors in Figure 4.2 with the regulated cascode MOS circuit[6].

The CWU in Figure 4.2 which consists of two transistors; M_W and M_{B1}. Transistor M_W operates in saturation mode and acts as a diode. Therefore, its input shows low resistance which is suitable for input current. Transistor M_{B1} is controlled by by transistor MC6 which in turn controlled by external digital signal. The input current signal will be stored as a charge in the gate capacitance of M_W. The amount of this charge is given by

$$Q = WLC_{ox}\left(\sqrt{\frac{2I_{in}}{\beta}} + V_T\right) \qquad (4.1)$$

where β is $\mu_n C_{ox}\frac{W}{L}$ in which *W, L, Cox*, and μ_n are width, length, gate capacitance, and electron mobility, respectively.

The current read unit (CRU) consists of two transistors M_R and M_B, Figure 4.2. Transistor M_{B2}, which is controlled by transistor MC6, provides enough current so that M_R is always in saturation.

The switch unit (SWI) uses two conventional MOS switch as shown in Figure 4.2. M_{S1} is for connecting the stored charge in the write unit to the input of the read unit. The other transistor, M_{S2}, is used to ground the read input when the current switch is off. Both transistors in the switch unit are controlled by a digital signal which is generated by the logic unit.

The controlled current source(CCS) consists of M_{C1}-M_{C6} which form a current source. This current source performs five kind of tasks:

- Provides enough current for the read transistors to be in saturation.
- Provides enough current for the write transistors to accept negative and positive input signal.
- Controls the amount of DC current by means of an external analog control signal.
- Controls the power dissipation of whole switch by means of a digital control signal.
- Balances the transistor current in the read unit so that the output current has no offset current.

Figure 4.3 gives a detailed description of the 1x1 current switch, which can operate in one or two phases as follows: When the clock is high(ϕ), the switches S1 is on, and S2 and S3 are off. At this point, the input current will be saved as charge in the capacitor of the CWU, Eq. 5.1. At the same time, the CRU regenerates the input signal in proportional to the charge stored in the write unit. The CRU and CWU are completely isolated when S2 and S3 turned on. Therefore, the output current will be zero until switches S2, S3 remained on($\bar{\phi}$). In this circuit, one CCS is used for the write and read units which in turn reduces power dissipation and area. No DC current flows through the write or read units when the switches S2 and S3 are on. Therefore, power dissipation is minimized when the current switch is off.

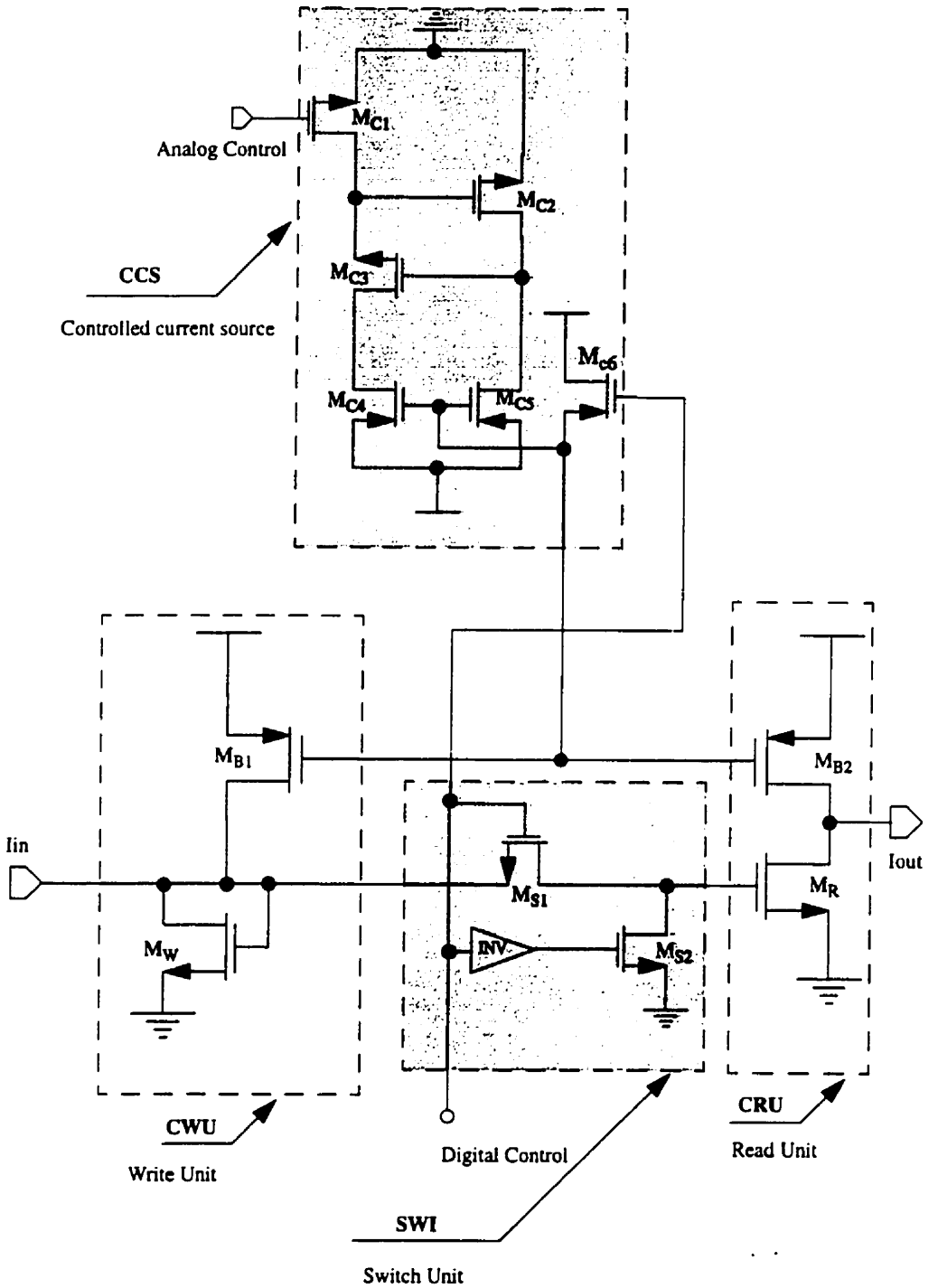


Figure 4.2 Circuit diagram of current mode switch.

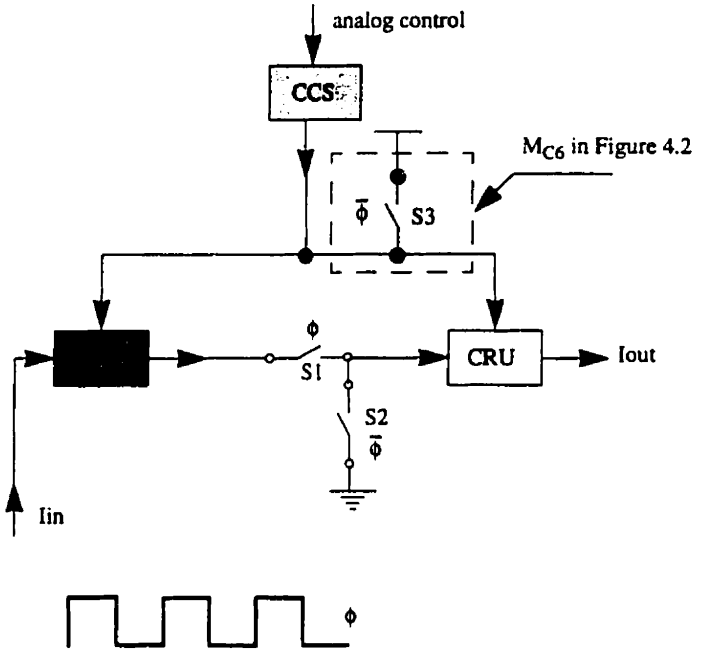


Figure 4.3 Circuit description of the 1x1 switch which shows its operation.

4.4.2 Analysis of Current Mode Switch

In order to characterize the voltage mode and current mode switch, the following two simple models in Figure 4.4 are used. If the input and output power of two switches are equal, then the on resistance of voltage mode switch can be related to circuit parameters of current mode switch by

$$R_{on} = \frac{(r_o + R_L)^2}{k^2 R_1 r_o^2} - R_L \qquad (4.2)$$

where, R_{on} is on resistance in voltage mode, r_o is the output resistance of current switch, and R_L is the load resistance.

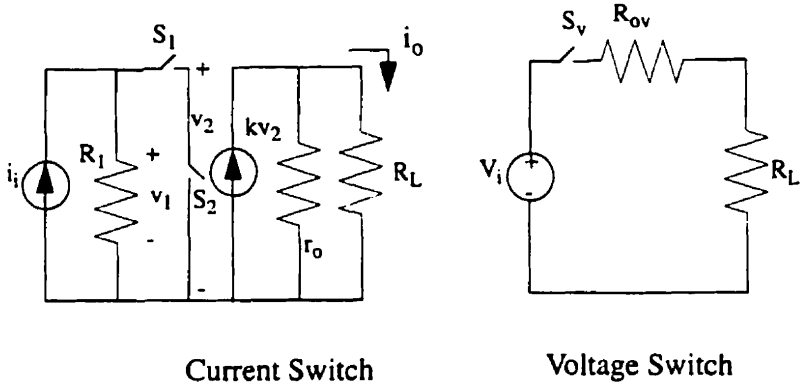


Figure 4.4 Models of current mode switch and voltage mode switch..

In general, This equation shows that on resistance in current switch can be modified by changing the circuits parameters. In most of the cases, when $r_o >> R_L$, then

$$R_{on} = \frac{1}{k^2 R_1} - R_L \qquad (4.3)$$

In Fig. 2 $k = 1/R1$, then

$$R_{on} = \frac{1}{k} - R_L \qquad (4.4)$$

K is equivalent transconductance of transistor circuit which is function of dc drain current. This means that on resistance of current switch can modified by changing the dc current.

Eq. 4.3 shows that the output resistance of current switch and the input transconductance have the main roles in the performance of current switch. In ideal case, *Ron* can be zero if $k = 1/R1$ and $r_o >> R_L$.

4.5 The Effect of non-ideal MOS Devices on the Current-mode Switch Performance

The performance of the current mode switch is based on the assumption of employing ideal MOS devices. However, a MOS device in practice is never ideal. A current mode switch suffers from degraded performance through analog errors resulting from non-ideal MOS transistor characteristics. In this section, the effect of non-ideal MOS will briefly discussed.

4.5.1 Channel Length Modulation

The channel length modulation is caused by the channel shortening of the MOS transistor. if the drain voltage changes, the output current of the switch also changes because of the channel length modulation. The change in drain voltage causes an error in the output current.

If $k = 1/R1 = g_m$, then the output current of the switch is given by

$$|i_o| = i_i\left(1 - \frac{g_o}{g_m}\right) \tag{4.5}$$

where g_o is the output conductance of the MOS transistor and g_m is the transconductance of the MOS transistor. Hence, the error Δi due to channel length modulation is given by

$$\Delta i = i_i\frac{g_o}{g_m} \tag{4.6}$$

The error in equivalent on resistance in voltage mode due to channel length modulation is given by

$$\Delta R_{on} = \frac{2g_o}{g_m^2} = \frac{\lambda}{\beta} \tag{4.7}$$

To reduce the effect of the channel length modulation, there are two solution. The first is to keep the drain voltage constant and second is to increase the output resistance of the current switch.

4.5.2 Switch Charge Injection

When a MOS transistor switch is turned on, a quantity of charge is stored in its channel. When the switch turn off, the charge is injected into its surrounding circuits nodes. In addition to the charge from the intrinsic channel, the charge associated with the feedthrough effect of the gate overlap capacitance also adds to the charge injection effect[7]. This distribution of charge creates an error voltage which produces an error in the output current. This error voltage depends on the ratio of equivalent capacitance in the drain and source terminal of MOS transistor and the switch turn-off time. If the ration of capacitance is equal one, then the channel charge is shared equally between two capacitance. If the error voltage is δV, then the error in the output current is given by[7]

$$i_o = \frac{\beta}{2}\delta V^2 + g_m \delta V + i_i\left[1 + \delta V \frac{g_m}{2I_D}\right] \tag{4.8}$$

Eq. 4.8 shows that switch charge injection error voltage produce a dc offset current and an ac current gain error. The error in the equivalent on resistance in the voltage mode is given by

$$\Delta R_{on} = \delta V\left(\frac{1}{2I_D} + \frac{2}{i_i}\right) \tag{4.9}$$

To reduce this error, the drain current of transistor must increase which in turn increases power dissipation.

4.5.3 Non-Ideal MOS Switch Effect on Settling Time of Current Mode Switch

To see the effect of the switch S1 and S2 on the performance of the current mode switch, it preferred to extract the frequency function of the current switch including the "ON" resistance of switch S1 and S2 in Figure 4.4. Figure 4.5 shows the small signal model of current mode switch.

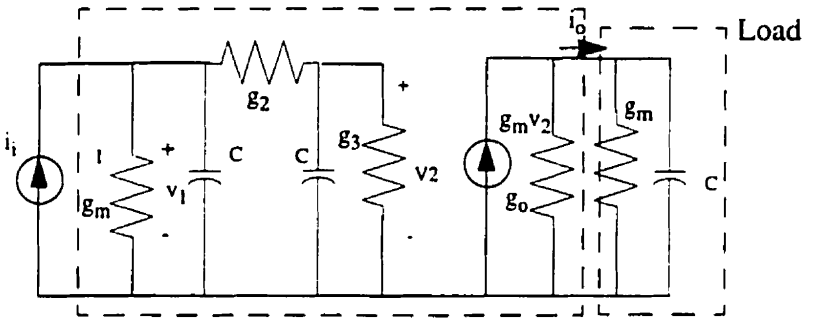


Figure 4.5 Small signal model of current mode switch.

The settling time of current mode switch depends on the its frequency response. The frequency response of switch is given by

$$\frac{i_o}{i_i}(s) = \frac{g_m g_2}{(1+s/p_1)(1+s/p_2)}$$
$$p_1, p_2 = \frac{1}{2Cg_m g_2}\left[(-(g_m+2g_2)) \pm \sqrt{g_m^2+4g_2^2}\right] \qquad (4.10)$$

where g_2 is conductance of switch S_2. In general where $g_2 << g_m$, the settling time is described by

$$i_o = i_i\left(1-e^{-1/\tau}\right) \qquad \tau = C/g_m \qquad (4.11)$$

For low frequency application, the effect of non-zero settling time error is not significant. However, for high frequency application, non- zero settling time error causes current distortion. To reduce the effect g_2 on the settling time, it is required to increase g_m which in turn reduces settling time. Figure 4.6 shows the frequency response of current switch.

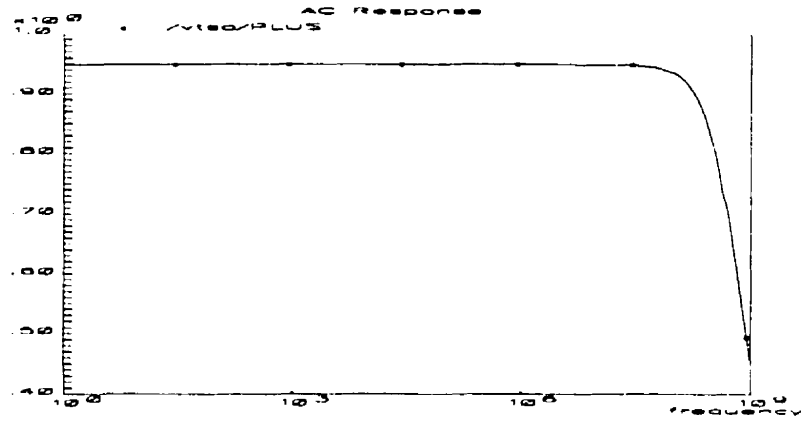


Figure 4.6 Frequency response of current switch.

4.5.4 Mismatch Effect

The process mismatch between transistors produces scaled output current errors. The mismatch between transistors could be in the threshold voltage V_T, the device ratio W/L, the process gain μCox, or in the channel length modulation λ. These mismatches create current gain error, dc error, and harmonic distortion.

4.6 Application

4.6.1 Current Mode Switch Array

The conventional switch matrix should allow the transfer of data from n inputs to m different outputs. In order to do so, the architecture shown in Figure 4.7 is proposed.

Suppose that we have n inputs, a matrix of $n \times m$ switches, and m outputs. CWU stands for current write unit, Y-control and X-control for cell addressing, V->I for voltage-to-current conversion and I->V for current-to-voltage conversion. The addressing should enable *1* to *m* possible communications between inputs and outputs.

Let us suppose that input *i* will communicate with host *j*. Then the line *i* is selected by X decoder and column *j* is selected by Y decoder. The information is transferred from *i* to j, passing through a current circuit which includes a switch and a read unit, *Cij*.

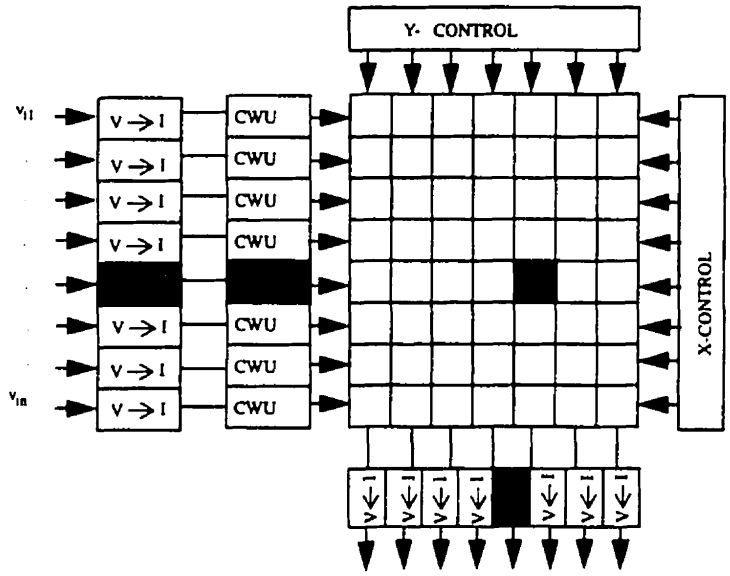


Figure 4.7 Architecture of current switch array.

4.6.2 Current Mode A/D converter

This design will be explained completely in Chapter 5.

4.7 Current Mode switch Implementation

Although this invention has the potential to be implemented in any conventional technology, like CMOS, GaAs, BiCMOS, or Bipolar, CMOS is still the preferred technology to design the switch. This choice allows high integration density and small size.

In order to verify the performance of the proposed switch, circuits have been fabricated by 1.2 μm, MITEL CMOS technology. The threshold voltages are 0.8 V for NMOS and -0.7 V for PMOS. In order to reduce parasitic elements and gate resistance, the transistors integrated with an inter-digit layout. Figure 4.8 shows the prototype die photo of current mode switch.

The proposed switch has been designed in two arrays; 1x1 and 2x2 with logic control which occupy 0.02 mm^2 and 0.15 mm^2 area, respectively.

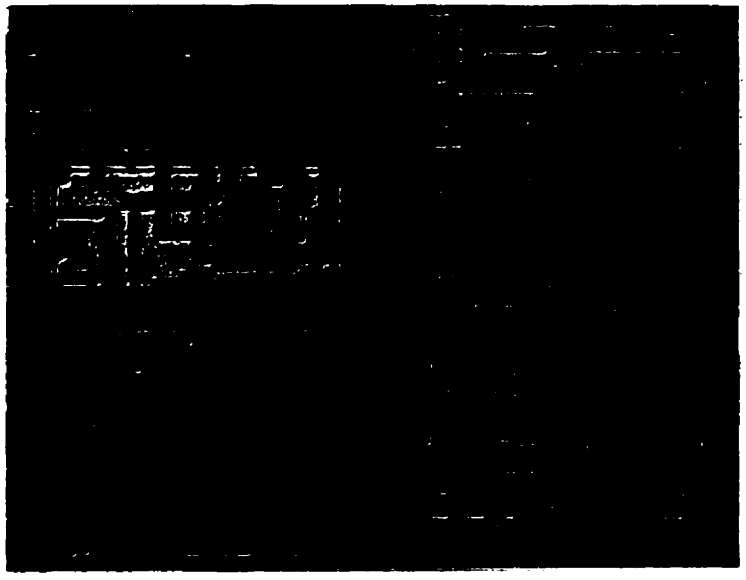


Figure 4.8 The prototype die photo of current mode switch.

4.8 Simulation and Experimental Results

To verify the performance of the current mode switch, the switch has been simulated and tested with MITEL 1.2 μm CMOS technology. The test has been performed in two condition DC and AC. In addition, matching problem has been considered in AC test. Figure 4.9 shows the test setup for the current mode switch.

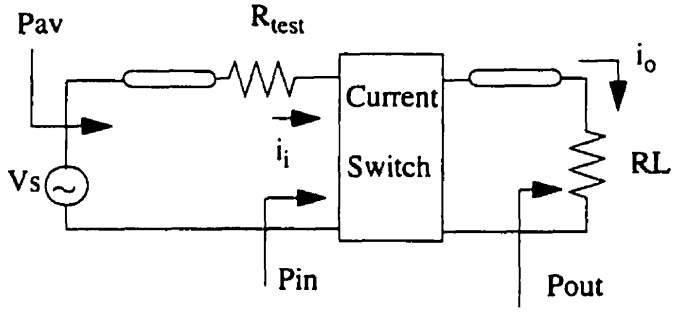
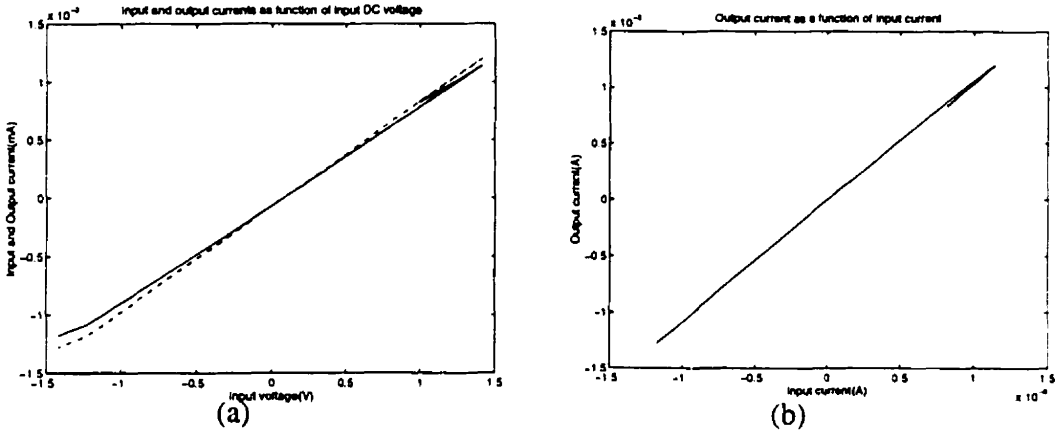


Figure 4.9 The test setup of

4.8.1 DC Test

In the first test, the single current switch is tested in DC situation. In this test, the power supply and logic level were fixed in +/-1.5 V. The current input was provided with a source voltage and input resistance of 1 KΩ. The output of the switch drives a load resistance of 100 Ω. The input voltage was varied from -1.5 V to +1.5 V. In this test, the isolation of the switch was also tested. It can be seen that the isolation in DC situation is more

than 100 dB. Figure 4.10 shows the output currents as a function of input voltage and input current.



(a) (b)

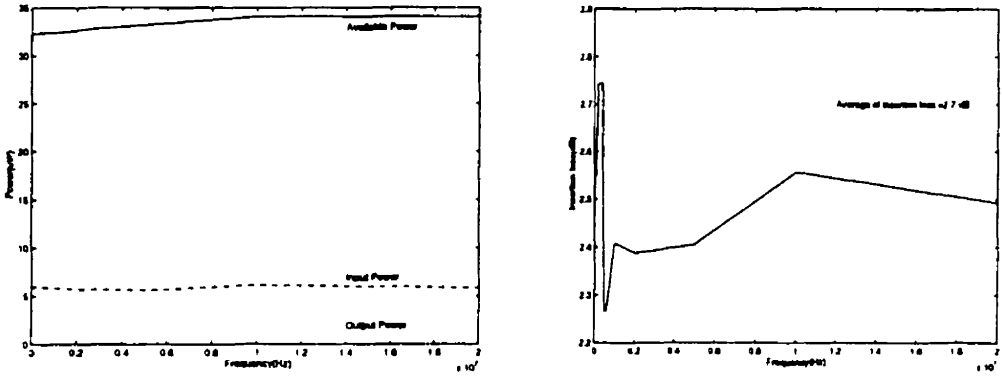
Figure 4.10 Output current as a function (a) input voltage (b) input current

4.8.2 AC Test

The switch has been tested under AC condition in four different modes.

4.8.2.1 Test of the Current Switch Without Matching Consideration

In the first step, A sinusoidal voltage with 0.6 V amplitude signal is applied to the switch input through 1 KΩ. The output current is measured through 100Ω. Then, the power(p_{av}), input power(p_{in}), output power(p_{out}) have been measured. Figure 4.11a shows 25% of total power is available in the input node of the switch. In other words, the rest of the power was dissipated in the 1KΩ resistance. Meanwhile the switch transferred most of its input power. Figure 4.11b shows the insertion loss in this test.

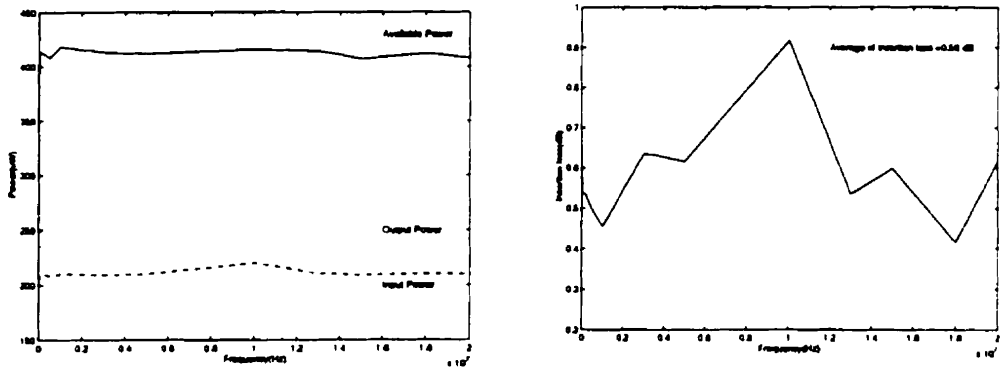


(a) (b)

Figure 4.11 (a) Power in different nodes of current switch without matching (b) Insertion loss of current switch without matching.

4.8.2.2 Test of the Current Switch with Matching Consideration

In the next step, the switch was tested with matching consideration. Here, the load was fixed with 200 Ω The input voltage applied through 200 Ω. The same test has been done to measure the power in different nodes and insertion loss. As shown in Figure 4.12a, 48% of the total power was transferred to the input of the switch which shows good matching. Meanwhile, the output power is little higher than of the input power. This is because of the gain of current switch which can be modified easily.



(a) (b)

Figure 4.12 a) Power in different nodes of current switch with matching (b) Insertion loss of current switch with matching.

Figure 4.12b shows the insertion loss in the current switch. It is clear that insertion loss in this case is less than that without matching consideration.

4.8.2.3 Transient Test of Current Switch with Matching

The switch was tested with the same condition as before except that the input frequency was fixed and the input voltage level was varied. Figure 4.13 shows the results of this test. The average of insertion loss is about 0.36 dB.

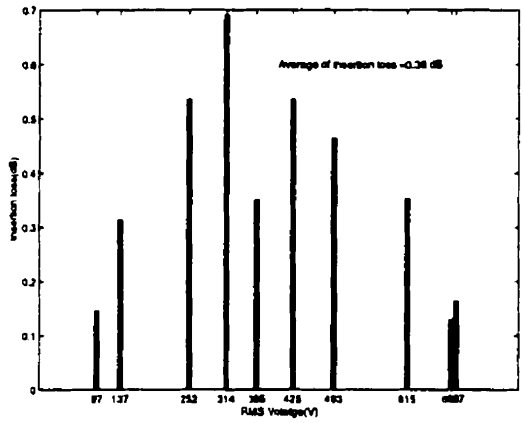


Figure 4.13 Insertion loss as function of different input.

4.8.2.4 Isolation Test of the Current Switch

The last test of the current switch was performed when the switch is off. This test is to find the isolation of the switch. Figure 4.14 shows the result of this test.

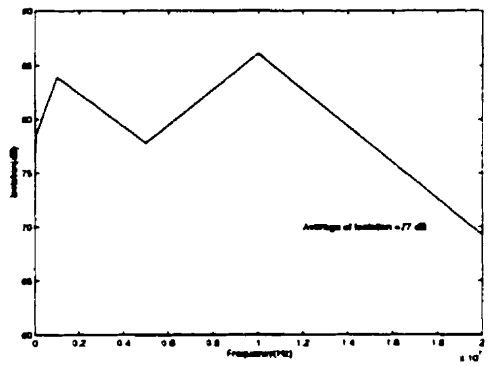


Figure 4.14 Isolation of the current switch.

4.8.3 Test of Switch Array 2 x 2

The switch array of 2 x 2 is tested under DC and AC condition. The result of DC test was similar to the single switch. On the AC test, a square wave was applied to one input and a sinusoidal signal applied to the there input. The array was switched between different inputs. The total results were satisfactory. Table 4.1 shows some of the final results of the current mode switch.

Table 4.1 : Test Results of current mode switch

Parameters	Symbol	value	unit
Insertion loss with matching	In	0.56	dB
Insertion loss without matching	In	2.7	dB
Isolation		>60	dB
Power Supply		VDD = +1.5, VSS = -1.5	V
Logic level	0 , 1	"1" = 1.5, "0" = -1.5	V
Power dissipation during On	$P(on)_{dis}$	13	mW
Power dissipation during off	$P(off)_{dis}$	5	mW
Turning on time	t_{on}	<40n	nS
Turning off time	t_{off}	>60	nS

4.9 Conclusion and Discussion

A switch in current mode for high performance and low voltage application has been presented. This switch has been designed and fabricated in 1.2 μm MITEL CMOS technology. The experimental results show that this switch can operate in better performance than a voltage mode switch. The following are the main conclusion based on the experimental and simulation results:

- ***Power dissipation***: Power dissipation in current mode switch can be less than that of similar design in voltage mode. Although, it should be noted that the current mode switch is an active switch and it can not compared with static voltage mode switch. Meanwhile, most of the power dissipation in switch array is related to the logic unit which is common in both modes.

- ***Isolation:*** Isolation in current mode switch is more controllable. This is because we isolated the input stage and output switch by a conventional switch. If this switch does not have enough isolation and some of the signal transferred to the output stage, this amount of the signal is not enough to drive the output stage. Therefore, the output stage still remain in off situation.

- ***Insertion loss:*** As we see from the first plots and experimental results, on resistance or insertion loss of current switch depends on the output resistance of output stage and DC bias current. The higher output resistance, the less insertion loss we have. The output resistance of the current switch is determined with output resistance of the current mirror used in switch. There are many techniques in order to increase the resistance of the current mirror. Therefore, the output resistance of the current mirror is high so that we can use Eq. 4.3. This means that the insertion loss can be changed by DC current. The best case is to set the DC current so that the input resistance of the switch is equal to the load. In other words, insertion loss can minimized as much as possible.

- ***Matching:*** In order to transfer most of the power to the input of the switch the input resistance of the current switch must be the same as source resistance(including cable and parasitic resistance of source). On the other hand, the load resistance and input resistance determined the insertion loss. Meanwhile, the load resistance determines the swing in the output current. Therefore, there is a trade off between these parameters.

Normally, the DC current is set based on the load resistance in order to reduce insertion loss. Then, an additional resistance which is series with input voltage modifies the matching.

- ***Speed:*** Speed is another potential of current switch. This properties is comparable with the speed of the voltage mode switch.
- ***Power dissipation when the switch is off:*** The current switch is an active circuit. Therefore, it is required some power during off. This power dissipation is very low compared to power dissipation of the other active circuits.
- ***Limited output swing:*** The potential of low insertion loss can limit the availability of the high current swing in the output. Therefore, there is a trade off between the on resistance and output swing.
- ***Limited input voltage level:*** If the current switch is operating with input voltage, the input level must be limited. This is because of the limited input current and matching problem.

In general, current switch is a new approach in order to have a high performance switch. This approach is comparable with the voltage mode switch. In most of the cased both approaches can complete each other. However, the current switch performance depends on its application.

4.10 References

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CHAPITRE V

Un nouveau convertisseur A/N "subranging" en mode courant pour des application à haute vitesse

5.1 Résumé

Dans le chapitre précédent, un nouvel interrupteur en mode courant a été proposé pour l'utilisation dans le convertisseur A/N en mode courant. De plus, nous avons mentionné que la technique en mode courant n'a pas besoin de circuits, ou de composants analogiques de hautes performances. Cependant, l'architecture et les algorithmes choisis jouent un rôle important dans la performance du convertisseur A/N mode courant, d'où la nécessité que l'architecture proposée dans le chapitre 3 soit utilisée dans le convertisseur A/N en mode courant.

Une nouvelle architecture en mode courant a été examinée pour les convertisseurs analogiques-numériques. Elle est décrite dans ce chapitre. Un convertisseur de haute résolution opérant à hautes fréquences a été développé. Il effectue la soustraction et la comparaison en parallèle. Le convertisseur fait une conversion de 2 bits au premier étage qui est suivi par d'autres étages similaires pour avoir un convertisseur analogique-numérique de 12 bits de résolution. Notons que la vitesse et la résolution dépendent de la précision du premier étage. Pour augmenter la précision, un miroir de courant avec contre-réaction a été utilisé comme soustracteur de courant. L'amplification normale du signal dans chaque

étage est évitée en additionnant les différents courants de référence dans chaque étage, ce qui réduit la non-linéarité due aux amplifications entre les étages. Le convertisseur en mode courant a été conçu et implanté avec la technologie CMOS 1.2 µm de MITEL. La tension d'alimentation était de 3 V. Le INL et le DNL sont approximativement 1.5 LSB et 1 LSB respectivement. La performance du convertisseur analogique-numérique montre un rapport signal sur bruit de 60 dB pour une fréquence d'entrée de 100 KHz. Ce qui veut dire que le nombre effectif de bits est 10. Lorsque la fréquence atteint 50 MHz, le rapport signal sur bruit baisse à 55 dB, ce qui présente un nombre effectif de bits de 9.

L'algorithme utilisé dans le convertisseur analogique-numérique en mode courant sera introduit dans la première section de ce chapitre. Le convertisseur analogique-numérique est présenté avec la matrice d'interrupteurs dans la deuxième section. La troisième section discute du miroir de courant ainsi que du comparateur de courant. La quatrième section discute les effets de non-linéarité et les effet des erreurs sur la performance. Finalement, à la dernière section du chapitre, les résultats des erreurs de non-linearité sont présentés. Notons que l'article proposé dans ce chapitre a été soumis au "Journal of Analog Integrated Circuits and Signal Processing".

Novel Current Mode Subranging A/D Converter for High Speed Application

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Note: This paper has been submitted for publication in the Journal of Analog Integrated Circuits and Signal Processing, Kluwer Publishing.

5.2 Abstract

A new current mode architecture for the A/D converter is presented in this paper. A high-resolution and high-speed converter has been achieved as a result of performing subtraction and comparison operations simultaneously. The converter performs a 2-bit conversion per stage followed by similar stages in order to obtain a 12-bit A/D converter. The speed and resolution depend on the accuracy of the first stage. In order to improve the accuracy, regulated current mirror with feedback is used as the current subtracter. Meanwhile, normal signal amplifying at each stage is prevented by scaling the reference current and summing the various signals in each stage. This causes the nonlinearity error sourced from interstage amplifier to be reduced. The circuit has been designed and implemented in CMOS *1.2* μm MITEL technology. The power supply is *3* Volts. The INL is about 1.5 LSB and the DNL is less than 1 LSB. The A/D performance shows a 60 dB signal-to-noise ratio with a 100 KHz input. This means that the effective number of bits is 10. When the input frequency increases to 50 MHz, the S/N ratio degrades to 55 dB, which in turn shows 9 bits as the effective number of bits.

5.3 Introduction

The advancement of CMOS digital technology is motivating designers to implement most of the signal processing functions in the digital domain. Signals in the real world however, are in analog form. Therefore, an analog-to-digital(A/D) converter is required to interface digital circuits to these analog circuits. Now, integrating the A/D converter with digital elements imposes some requirements on its design such as compatiblility with available technology, a high sampling rate and the use of only a small portion of the total chip area.

Switched-capacitor(SC) circuits have been used as a low cost and fully integratable method of creating the A/D converter. Simple SC circuits consist of a high gain operation amplifier, switches, and a precision linear capacitor. Accuracy depends on the capacitance ratio. The realization of floating capacitors with high ratio accuracy requires more fabrication steps than the standard digital CMOS process. The A/D converter must, therefore, be realized in a process without reliance on closely matched or high accuracy resistors or capacitors.

To improve the sampling rate, the time required for the voltage signal to settle on both the circuit capacitor and the parasitic capacitors at the various nodes must be reduced. This objective can be achieved if the signal is in current mode, which tends to reduce voltage swing and higher operating speeds.

Current-mode circuits are rapidly becoming a topic of wide interest[5-8]. The current-mode technique (in which the signal is essentially processed in the current domain) offers a number of advantages. Generally, current mode circuits do not require amplifiers with high voltage gains, thereby reducing the need for high-performance amplifiers. At the same, time current-mode circuits generally do not require either resistors or capacitors,

and, when capacitors are used to store the signal, they need not display either good ratio matching or good linearity. Therefore, current-mode circuits can be designed almost exclusively with transistors, making them fully compatible with most digital processes. The current-mode circuit also has a low power supply voltage requirement, since it uses wideband current mirrors as amplifiers as opposed to switched-capacitor circuits which employ operational amplifiers.

Although the current mode technique may reduce the need high performance analog circuits and components, still the architecture and algorithm in A/D operation still play a significant role in A/D performances.

The algorithm for the current mode A/D converter is considered in the first part of this chapter. Then, the current mode A/D converter is introduced through a current mode switch array. The design considerations of current mirrors and current comparators are discussed in the next section. Following this, the effects of nonideality and errors are presented. Finally, the result of nonlinearity errors is presented.

5.4 Algorithm for the Current-Mode Subranging A/D Converter

The algorithmic A/D conversion for a 2-bit cell is shown in Figure 5.1. The input current, *Iin*, which can take any value between zero and the reference current, *Iref*, is first subtracted from, and compared with, three kinds of reference current, *3lsb, 2lsb, 1lsb*. The output of the comparators will be encoded in order to obtain two MSBs, *D1D0*. To amplify the signal, the subtraction results are added to one of the correct reference currents. The correct reference current will then be selected by the logic circuit. Figure 5.1 only demonstrates this for a 2-bit cell, which mainly consists of three comparators, four subtracters and two kinds of reference current.

The function of sample and hold and subtraction is performed by a current memory cell. Figure 5.2 shows the general circuit for current, subtraction, S/H, and comparator(SS/HC). The input and reference currents enter at node #1 in Figure 5.2. Then, the subtraction of these currents is sampled and held by current memory which consists of M1, M2 and switch S1. The subtracted signal, the current in the drain of M3, is compared with zero by a current comparator(CC). The output of the comparator is latched and sent to the digital section. The drain current of M2 is an analog current proportional to the difference between the input current and the reference current. The function of the comparator is performed during the hold time. The output of this cell is in nodes #2 and #3.

To implement a 2-bit cell A/D converter based on the flow chart in Figure 5.1 and basic current mirror, the circuit shown in Figure 5.3 can be used. Here, k_i and k_r are the ratio of width to length of the input transistor and reference transistor respectively. The input current, node # 4, is replicated by 4 transistors, which is shown in the upper section of Figure 5.3. The reference current, node # 5, is multiplied by 3, 2, 1, -6, -2 and 6. Three of these reference currents will constitute the input of three SS/HC cells. The other reference currents will be used to correct the analog current at node #8. Finally, one analog current and two digital signals will constitute the output of this cell, nodes # 6, 7 and 8.

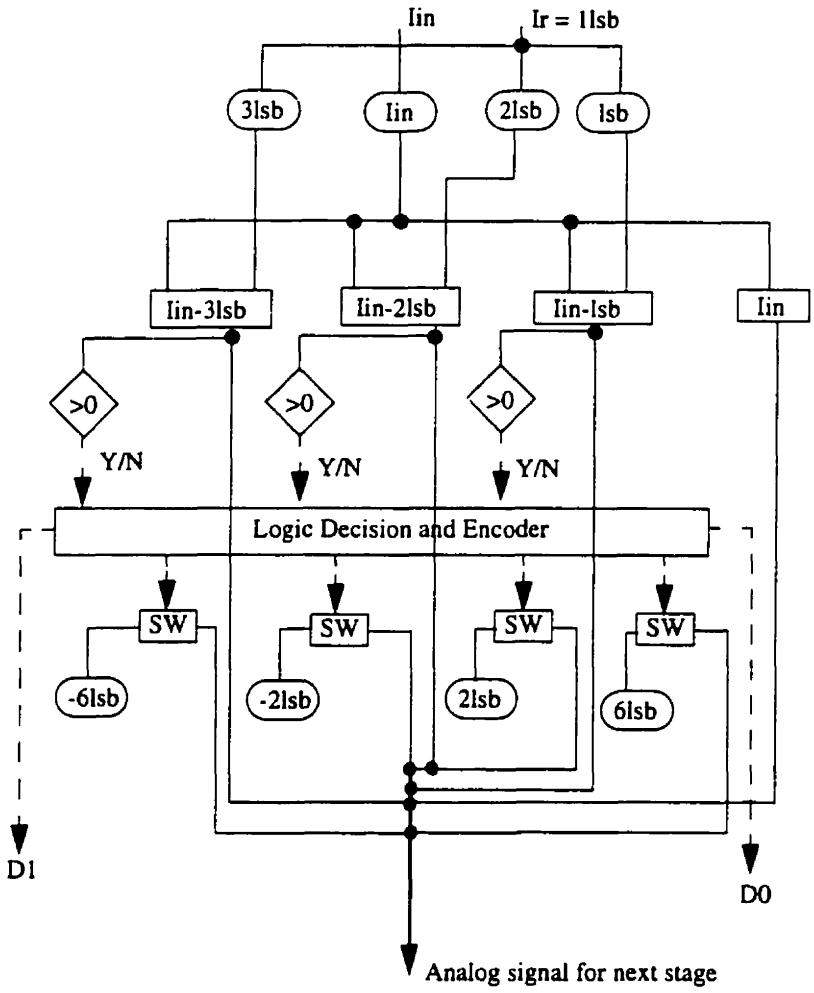

Figure 5.1 Flow chart of proposed A/D converter.

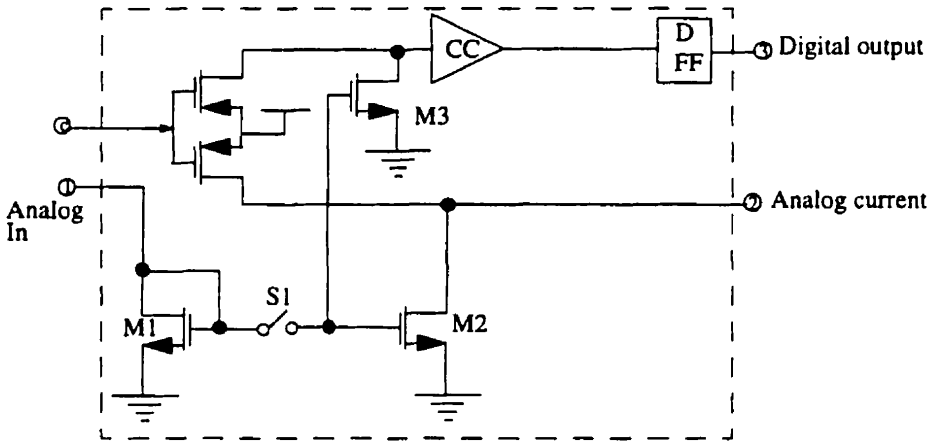

Figure 5.2 The SS/HC cell which performs subtraction, S/H and the comparator function.

To produce 12-bit A/D converter, 6 bit cells are cascaded with the analog current output of one cell connected to the analog current input of the following cell, as shown in Figure 5.4. Here, the reference transistor is shared by all the 2-bit cells.

5.5 Design of Current Mode A/D Converter With Current Mode Switch Array

In Chapter 4, it was shown that a current mode switch array can be used for transferring the current signal from one stage to another. The current mode switch array has shown satisfactory results compared to the voltage switch array. Therefore, the current mode switch array is preferred for the architecture of the current mode A/D converter. Figure 5.5 shows the architecture of the current mode A/D converter using a 2x2 current mode switch array. This architecture performs the same function as in Figure 5.3.

In this architecture, the output of the encoder is used to address the switch array. Therefore, the logic unit which is used in the structure in Figure 5.3 is not required in this

architecture. In addition, the subtracted current is multiplied by 4 is by summing the output currents of the switch arrays.

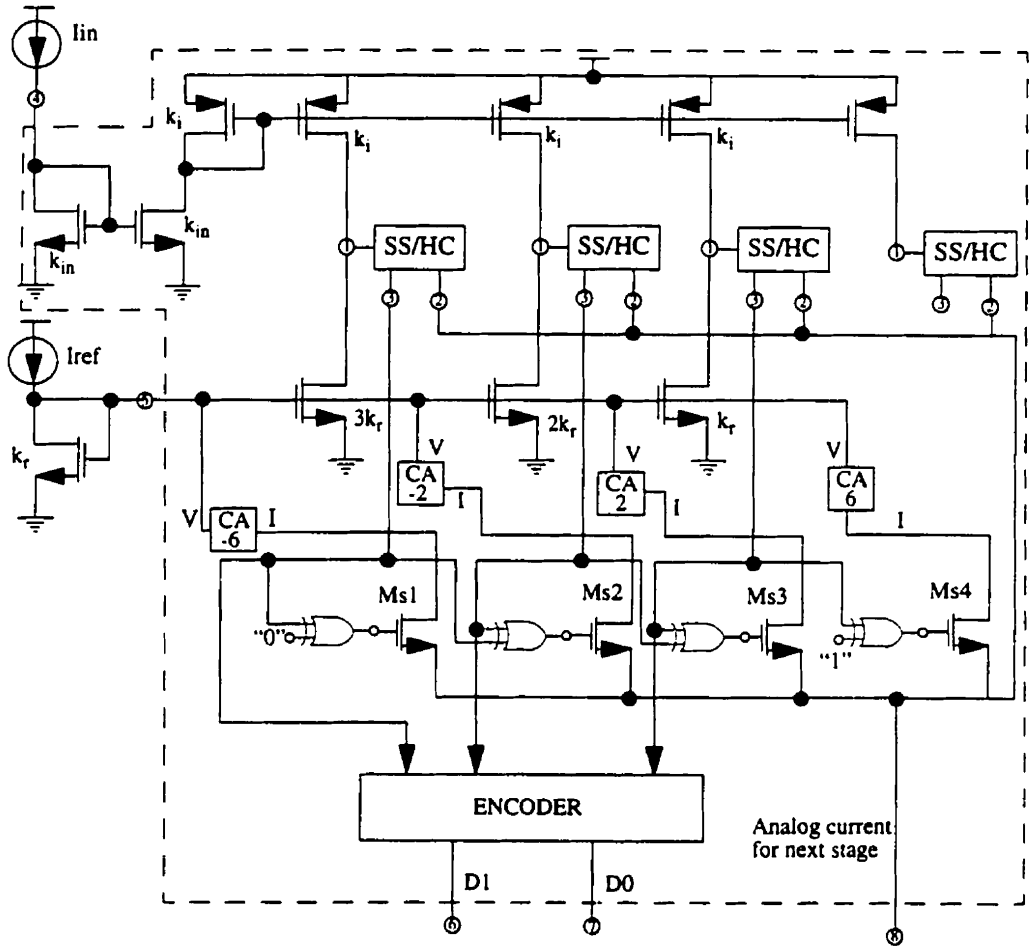

Figure 5.3 Bit cell for implementing 2-bit current mode subranging A/D converter

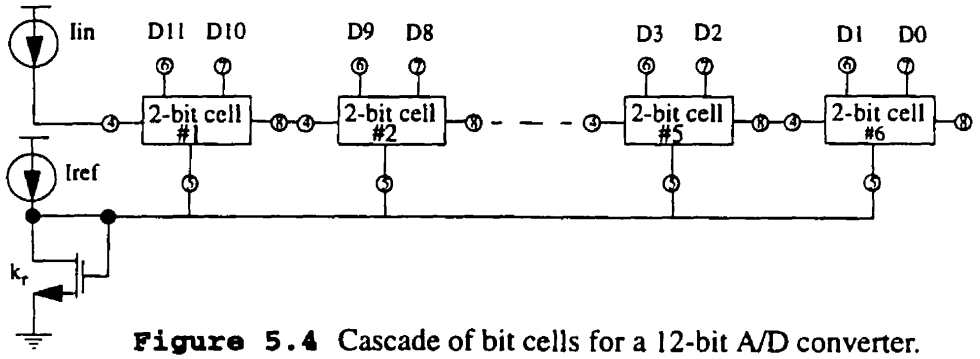

Figure 5.4 Cascade of bit cells for a 12-bit A/D converter.

5.6 Current Mirror as Critical Circuit In Current-Mode A/D Converter

Speed and accuracy are the two main advantages of the current-mode approach. The current-mode approach relies on the use of a current mirror to achieve higher performance. The current mirror is therefore a basic circuit in the current-mode A/D converter. Its performances affect the performance of the A/D converter.

Different kinds of current mirror, like the simple current mirror, the wilson current mirror, and the cascading current mirror, have been studied and explained in a textbook[19]. Each of these kinds of current mirror is suitable for a special kind of application. The Current mirror with a high output resistance and good current matching is suitable for the current-mode A/D converter.

A regulated-gate cascode current mirror is a good current mirror for the proposed current-mode A/D converter. Figure 5.6 shows the structure of a regulated current mirror. Transistors M1, M2, and M3 act as "super transistors" with high output resistance and swing voltage[3]. The DC current I_{B0} is for maintaining the transistors M1 and M4 in sat-

uration. The feedback topology controls the gate voltage of cascode transistor(M2) and regulates the current over the operating range.

There are some parameters which characterize current mirrors. Here, the parameters that affect the performances of current-mode A/D converters are addressed.

- Signal swing (I_{ss}): the allowable input current signal that can be applied to current mirrors while maintaining proper circuit operation.
- Signal-to-noise ratio(SNR): the ratio of the maximum signal power to the worst case noise power; this parameter limits the accuracy of the current mirror.
- Minimum bandwidth (ω_{min}): the minimum bandwidth required for the current mirror to operate properly; ω_{min} is determined by the settling time of the current mirror.
- Power dissipation (P_{dis}): the average consumed power; it is the product of average current times the supply voltage.
- Output resistance (r_{out}): the ratio of the output voltage to the output current when the input voltage is zero.

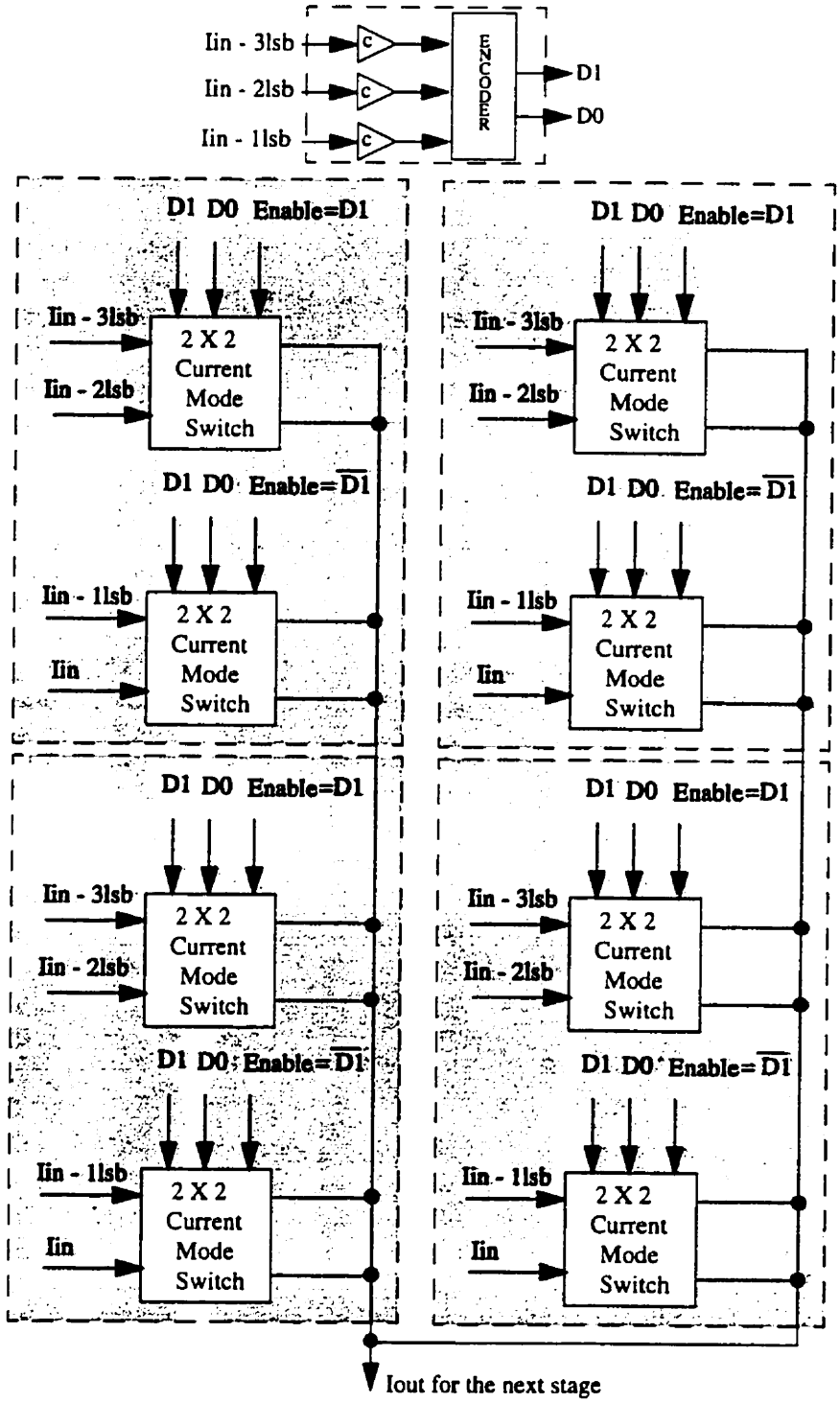

Figure 5.5 The architecture of 2-bit current mode A/D converter wit current mode switch

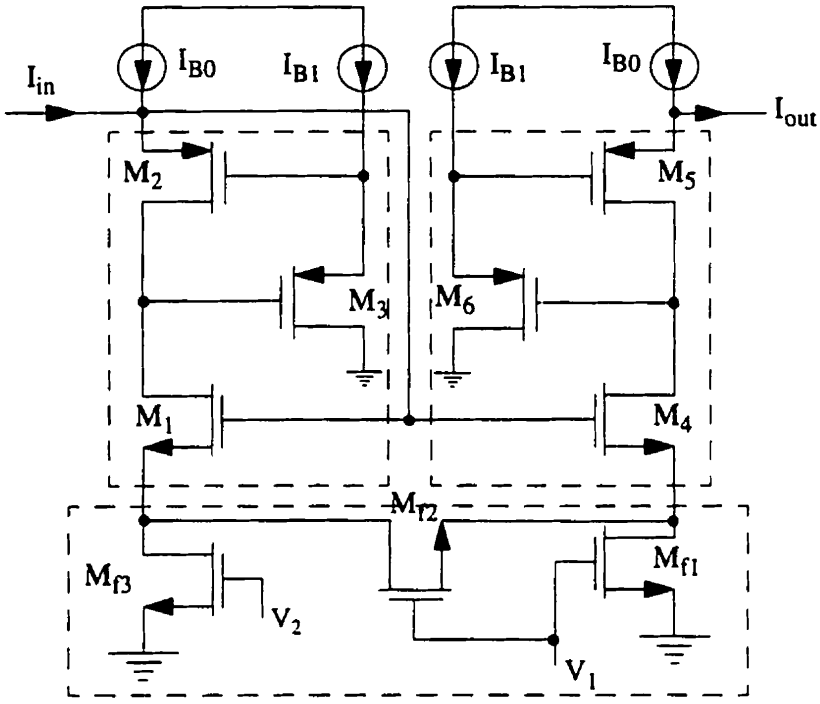

Figure 5.6 Regulated cascode current mirror.

If all transistors operate in saturation mode, then the drain-source voltage of M1 is constant and is controlled by DC current I_{B1}. Hence, the maximum drain current of M1 is determined by a constant drain-source voltage. This maximum current is

$$I_{D(max)} = \frac{\beta_m}{2}\left[V_T + \sqrt{\frac{2I_{B1}}{\beta_c}}\right]^2 \qquad (5.1)$$

where β_m is the conductivity parameter of M1, M2, M4, and M5, and β_c is conductivity parameter of M3 and M6. It is clear that the minimum drain current is zero. Therefore, Eq. 5.1 determines I_{ss}.

The step response can give some information about the settling time. The step response depends on the model of transistors. In other words, the amplitude of the current

in most of the circuit is large enough not to use a small signal model. An extensive analysis of the current sampler is performed in [1]. The settling time, t_s, for a current step from I_1 to I_2 with an allowable settling error of ε is

$$t_s \approx \frac{C_h}{\sqrt{2I_2\beta_m}} \ln\left|\frac{I_1 - I_2}{\varepsilon}\right| \tag{5.2}$$

where C_h is the total capacitance at the gate of M1.

Eq. 5.2 shows that the final step value plays a much greater role than the initial value in determining the current mirror's step response. A bias current, I_{B0}, is used to reduce settling time when the input current is zero. Therefore, the worst case of the settling time is determined by the minimum current of I_2 which is now I_{B0}. Then the maximum settling time is

$$t_{s(max)} \approx \frac{C_h}{\sqrt{2I_{B0}\beta_m}} \ln\left|\frac{I_1 - I_{B0}}{\varepsilon}\right| \tag{5.3}$$

Eq. 5.1 and Eq. 5.2 state that the settling time and output swing can be controlled by I_{B0} and I_{B1} independently.

This means that the minimum bandwidth, ω_{min}, is determined by the inverse of the coefficient of Eq. 5.3. This coefficient is the product of the inverse of the minimum transconductance and holding capacitance.

$$\omega_{min} = \sqrt{2\beta_m I_{B0}}/C_h = g_{m1(min)}/C_h \tag{5.4}$$

Based on Eq. 5.4, a non-zero I_{B0} can increase the minimum bandwidth but it will also decrease the signal swing. At the same time, power dissipation, $V_{DD}(I_{B0} + I_{B1})$, also increases. Therefore, there is a trade-off between speed, maximum swing and power dissipation.

The main sources of noise in Figure 5.6 are I_Bs, and M1 and M2 channel noise. A MOS transistor, since the channel material is resistive, exhibits thermal noise, and this is the major source of noise. This noise is defined as

$$\overline{i_{ch}^2} = \frac{8KTg_{m1}}{3}\Delta f \tag{5.5}$$

where Δf is noise bandwidth ($g_{m1}/4C_h$). By assuming that $g_{m1} = g_{m4}$, the total noise in the output is

$$\overline{i_{tot}^2} = \frac{4KTg_{m1\,(max)}^2}{3C_h} = \frac{8}{3}\frac{\beta_m kT}{C_h} I_{D\,(max)} \tag{5.6}$$

By assuming sinusoidal input with amplitude $I_{ss}/2$ and Eq. 5.1, S/N of the current mirror is given by

$$S/N = \frac{3}{128KT} C_h \left[V_T + \sqrt{\frac{2I_{B1}}{\beta_c}} \right]^2 \tag{5.7}$$

The output resistance of the regulated cascode mirror is given by

$$r_{out} = r_{o1} r_{o2} r_{o3} g_{m2} g_{m3} \tag{5.8}$$

By applying a feedback around the mirror, it is possible to reduce the error in the output current without affecting the other parameters. Figure 5.7 shows the output current

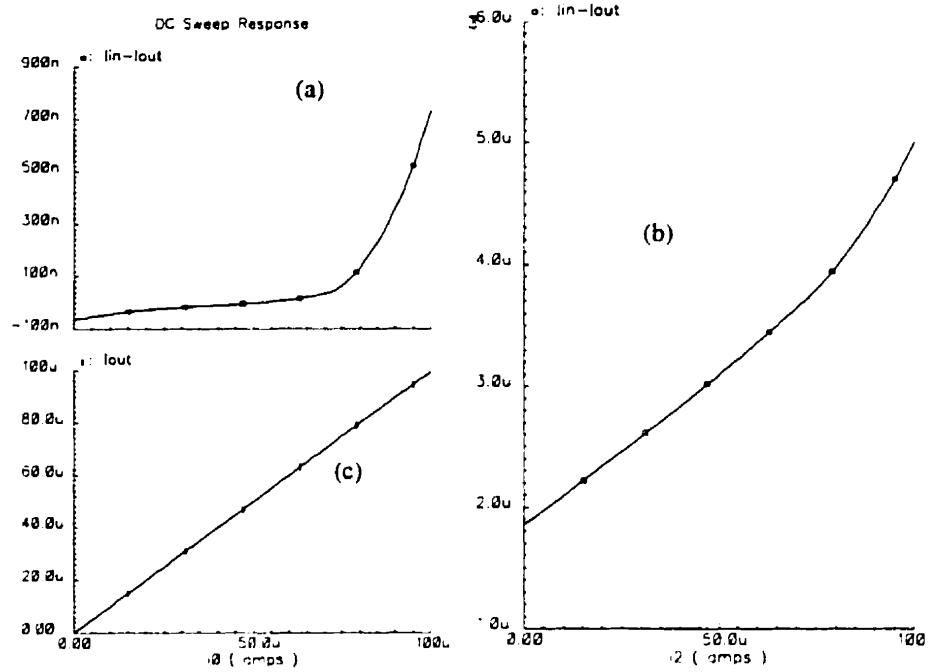

Figure 5.7 : (a) The error in output with feedback (b) The error in output without feedback (c) The DC characteristic of the proposed current mirror.

error with and without a feedback circuit. Figure 5.8 shows that the feedback doesn't have any effect on the delay, transient and frequency response of the cell.

5.7 Current-mode Comparator

In an A/D converter, comparators are used to quantize the threshold signal. Previously, it was difficult to directly compare one current level with another. For this reason, a plurality of current levels are conventionally converted into corresponding voltage levels by using resistors. The voltage levels are then compared by a voltage comparator. The problem with this method is that, the current levels change depending on the resistors used. Thus, a current level cannot be determined with any greater accuracy. When the mode of operation is current, it is preferable to have all signals in current mode.

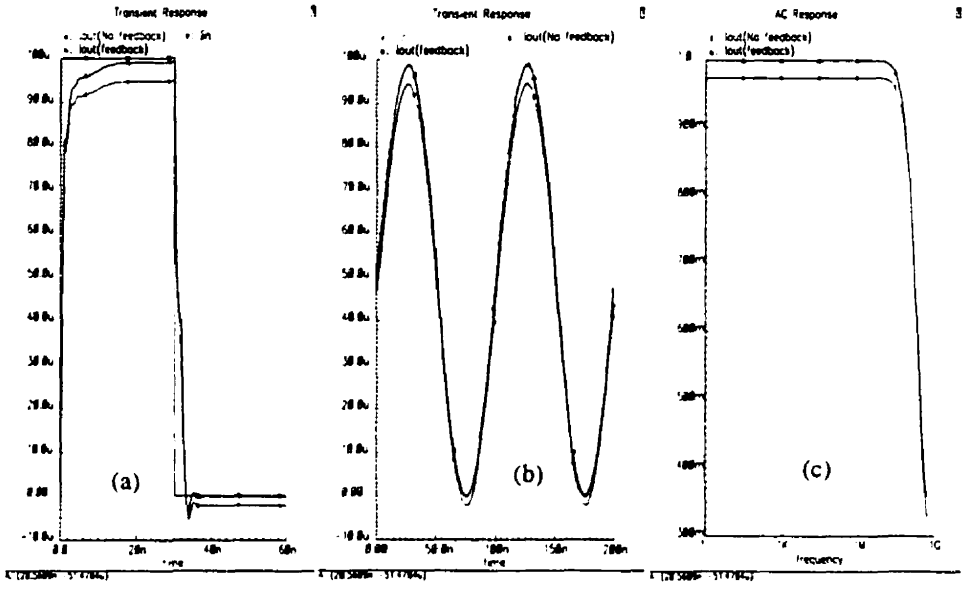

Figure 5.8 The response of regulated current mirror showing: (a) delay (b) transient response (c) frequency response.

A few kinds of comparators have been proposed[12],[13],[15],[17]. In the first generation of current comparators high resistance current mirrors are connected as a class AB stage[13],[15]. This kind of comparator amplifies small differences in input current to large variations in output voltage. The high output resistance will also reduce the frequency response of the comparator which in turn degrades its speed and resolution. The other current-mode comparator is a current mirror with positive feedback[17]. This comparator, however, has a signal dependent input resistance, and no control of the bias current exists. This comparator normally uses high power dissipation. In order to improve the accuracy of the comparator, offset compensation is used[12],[14],[16]. Although, this technique improves accuracy, is required another step for offset compensation.

In this section, a CMOS current comparator circuit is presented. Analog design techniques are used to develop an output voltage that indicates whether or not an input current exceeds the comparators threshold current. This current comparator is designed based on A/D converter requirements.

5.7.1 Performance Metrics

There are some parameters which describe the performance of comparators. These parameters are common to both voltage mode and current mode. The following are the important ones:

- *Resolution:* the minimum input difference that yields a correct digital output. It is limited by the input-referred offset and noise of subcircuits in comparator.
- *Comparison rate:* the maximum clock frequency at which the comparator can recover from a full-scale overdrive and correctly respond to a subsequent 1-LSB input.
- *Dynamic range:* the ratio of the maximum input swing to the minimum resolvable input.

5.7.2 Schematic of Proposed Current Comparator

Figure 5.9 shows the schematic of the proposed current comparator. It consists of an inverter and a CMOS buffer. When the clock set at high, the comparator is inactive and its positive output is low. When the clock set at low, the comparator output is active and its voltage depends on the current input. The switches between the comparator and output inverters make the comparator operates with the clock.

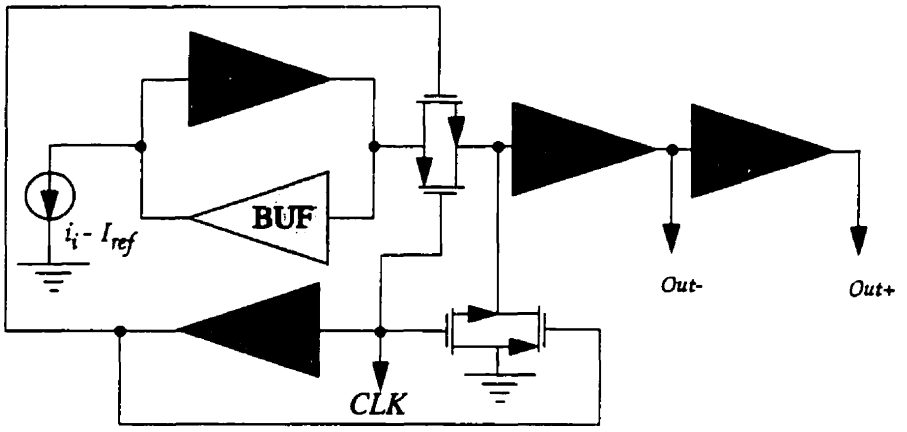

Figure 5.9 Schematic of CMOS current comparator.

5.7.3 Analysis of Current Comparator

The simplest current comparator is a CMOS inverter with current input and voltage output. The simple structure of the inverter motivated us to improve this structure in order to make it operate as a high speed and high resolution comparator. For this purpose, the performance of a simple inverter comparator (ICOM) must be compared with that of a buffered inverter comparator (BCOM).

The most important parameter in these two structures is the comparator delay. Their delays must therefore be analyzed in depth. Most of the proposed delay analysis of the CMOS inverter is based on applying the input voltage in the form of a step function. In other words, there is no delay in the input signal. Based on this assumption, the time required for turning on the NMOS transistor is zero.

The analytical response we derive is based on the Shichman-Hodges model of the transistor[2]. The objective of the analysis is to determine the delay of the current compar-

ator when we apply a step input current to the input. The current comparator is shown in Figure 5.6. We assume that the current in the PMOS is zero. The input of the comparator consists of a resistance, R, and a capacitance, C_g. The input current will charge the capacitance by the input time constant, $\tau_i = RC_g$. Therefore, the gate-source voltage will be written as follows:

$$V_{gs}(t) = RI_i\left(1 - e^{-t/\tau_i}\right) \tag{5.9}$$

where I_i is the size of the current input step.

The NMOS transistor requires time to transfer from OFF to SAT region, t_s. This time can be found by Eq. 5.9 when $V_{gs}(t) = V_T$:

$$t_s = \tau_i \ln\left(\frac{RI_i}{RI_i - V_T}\right) \tag{5.10}$$

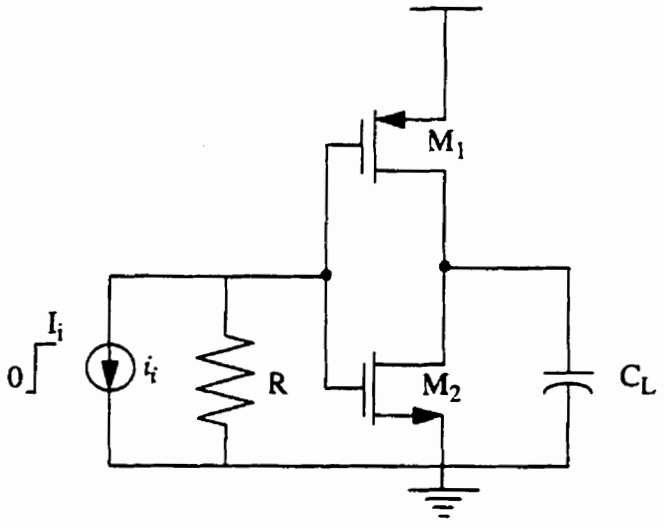

Figure 5.10 Simple CMOS current comparator.

The delay time for saturation and for the linear region can be expressed by[2]

$$t_L = \frac{n}{\sigma(1-n)^2} + \frac{Ln(19-20n)}{2\sigma(1-n)} \qquad n = V_T/V_{DD} \qquad \sigma = \beta V_{DD}/C_L \qquad \textbf{(5.11)}$$

The total delay is the sum of t_L and t_s in Eq. 5.11 and Eq. 5.10. Hence, the total delay mainly depends on τ_i, V_{DD}, C_L and W/L.

The speed of the comparator usually depends on the delay and the size of current amplitude. The delay in Eq. 5.10 mainly contributes to the speed of the comparator. In the simple inverter comparator, the input resistance is high. Therefore, the expected delay is high. In a buffered comparator, the resistance R is replaced by a CMOS buffer as in Figure 5.6. This buffer can have two jobs. First, it reduces the input resistance which in turn decreases the delay. Secondly, it increases the output resistance of the inverter. The simulation results show that the improvement in delay is from 50 nsec to 10 nsec, Figure 5.12. Figure 5.13 shows the propagation delay of the comparator as a function of the input current signal.

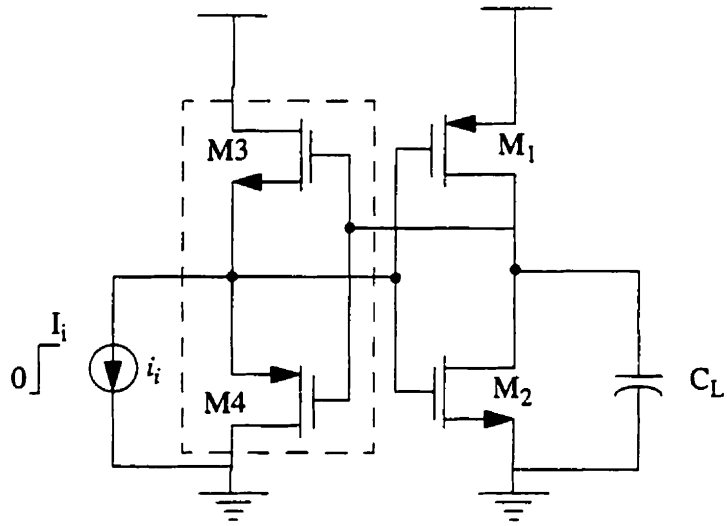

Figure 5.11 Simple CMOS current comparator with buffered.

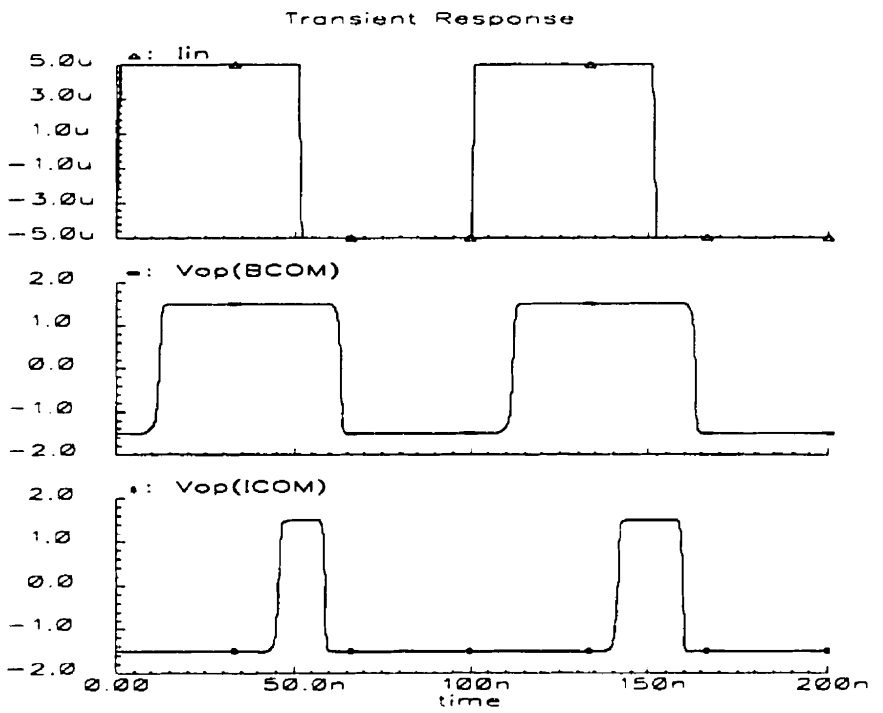

Figure 5.12 The pulse response of comparator showing the delay of comparator.

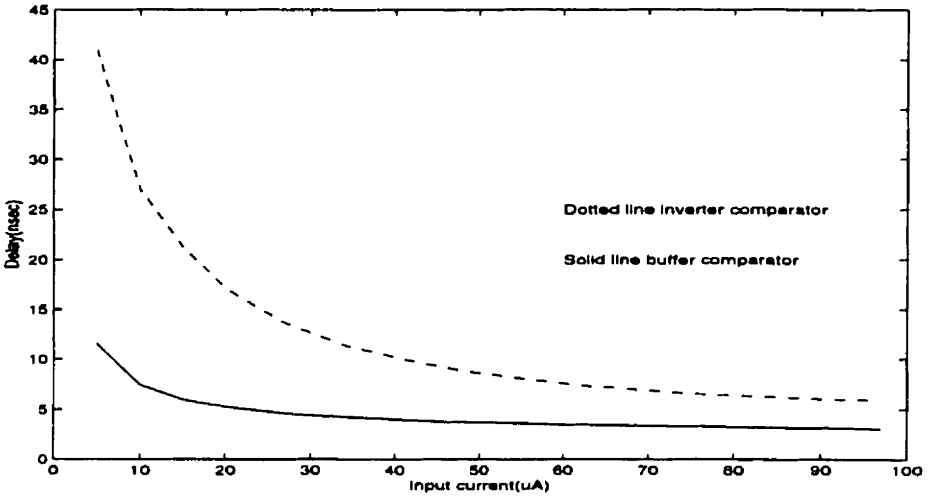

Figure 5.13 The delay of comparator as a function of input current.

The resolution of the current comparator depends on the transresistance of the comparator. One DC characteristic of the comparator is shown to be resolution less than 50 nA, Figure 5.14a.

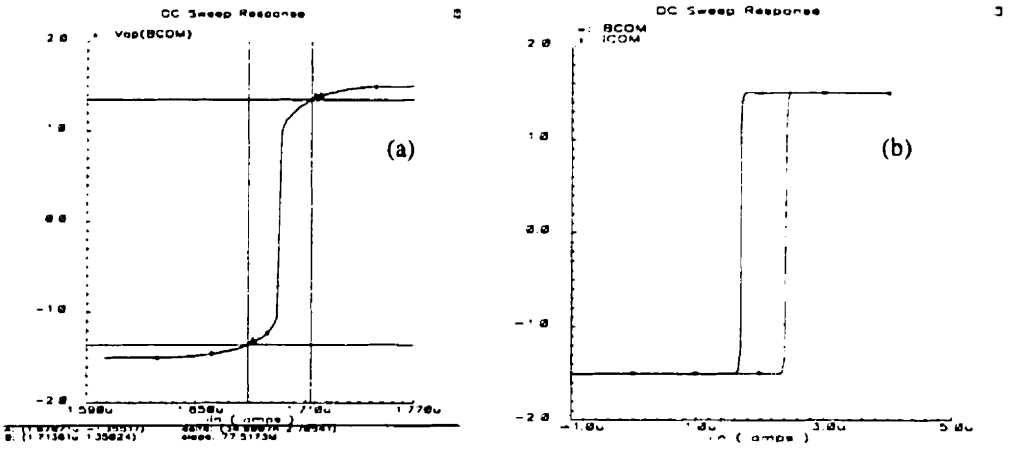

Figure 5.14 The DC characteristics of comparator: (a) the resolution and (b) offset current.

The offset current depends on the mismatch between the transistors. In the ideal case, both the PMOS and NMOS drain currents are equal, when the input current is zero. The offset current is related to the offset voltage. The offset voltage in a current comparator is given by

$$v_{os} = V_{DD}\frac{1-p}{1+p} - V_t\frac{n-p}{1+p} \qquad p = \sqrt{\frac{1+\lambda V_{DD}}{k(1+m\lambda V_{DD})}} \tag{5.12}$$

$$\beta_P = k\beta_N \qquad \lambda_P = m\lambda_N \qquad V_{tP} = nV_{tN} \tag{5.13}$$

where k, n and m are mismatch parameters. The offset current of the proposed current comparator is about 1.6 μA, which is half that of the simple inverter comparator (Figure 5.14b).

The ability of a comparator to respond very fast to an input signal can play a crucial role in the design of a current mode A/D converter. The objective is to perform comparison and subtraction simultaneously. This requires that the comparator show a good performance with a high slew rate input signal. Figure 5.15 shows the response of a current comparator to a current signal with a slew rate of 0.2 *μA/nsec* without any clock. Figure 5.16 shows the comparator response with clock system.

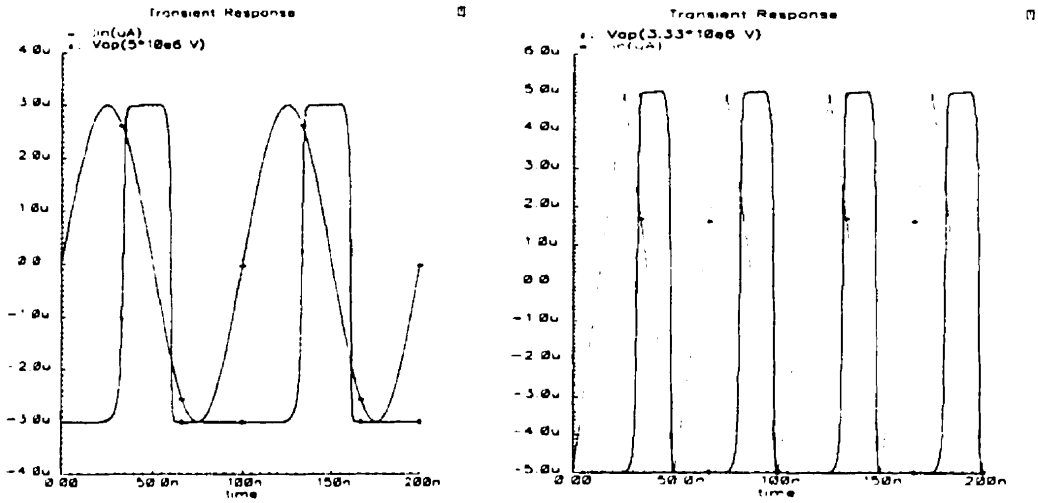

Figure 5.15 The response of a buffered comparator without any clock.

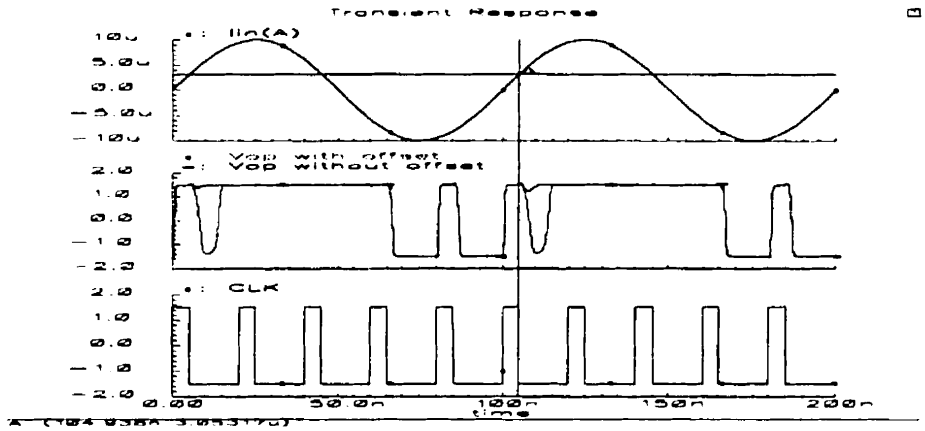

Figure 5.16 The response of a buffered comparator with clock..

5.8 Analysis of Error and Nonlinearity

5.8.1 Error in Accuracy

There are two main sources of error which affect the accuracy of the current-mode A/D converter; output resistance and the mismatching of devices.

5.8.1.1 Error in Accuracy Due to Output Resistance

If all 2-bit cells are similar, then the analog output of a cell is connected to a gate to drain the connected transistor, as shown in Figure 5.17. The input current of a 2-bit cell,

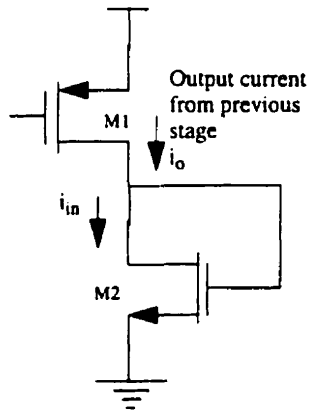

Figure 5.17 Model used for error analysis.

i_{in}, cab be expressed by

$$\frac{i_{in}}{i_o} = \frac{g_{m2} + g_{o2}}{g_{m2} + g_{o2} + g_{o1}} \tag{5.14}$$

where g_{m2} and g_{o2} are transconductance and output conductance of M2 and g_{o1} is the output conductance of M1.

To see the effect of output resistance on the current error, the reduction in current mismatch can be expressed by

$$\frac{\Delta i}{i_o} = \frac{g_{o1}}{g_{m2} + g_{o2} + g_{o1}} \tag{5.15}$$

Eq. 5.14 and Eq. 5.15 states that g_{o1} and g_{o2} should be as small as possible. In addition, g_{o1} should be smaller than g_{o2} in order to reduce current error. If this error is less than half the LSB, then the limit of output resistance on resolution is given by

$$N = \frac{\log (g_m/g_o)}{\log 2} - 1 \tag{5.16}$$

Here, it assumed that both transistors have the same output conductance. In a regulated current mirror, Eq. 5.16 can be modified as a function of power supply

$$N = 3.3\log\left(\frac{V_A}{\sqrt{\frac{2I_{B1}}{\beta_c}} + V_T}\right) \tag{5.17}$$

$$N = 3.3\log\left(\frac{V_A}{V_{DD}/2 + V_T}\right) \tag{5.18}$$

Using Eq. 5.18 for a V_{DD} of 3 Volts, maximum accuracy will be about 5 bits. Therefore, it is required that M1 show a very high resistance so that the ratio g_m/g_o in Eq. 5.16 increases.

5.8.1.2 Error in Accuracy Due to Mismatching

In order to see the effect of mismatching on accuracy, the mismatch in the output current of simple current mirror must be considered. The results of the simple current mirror can be applied to the other current mirrors. The mismatch in the output current mirror is expressed by

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\sqrt{2}\Delta\beta}{\beta} - 2\Delta V_T\sqrt{\frac{\beta}{I_{in}}} \tag{5.19}$$

where $\Delta\beta$ and ΔV_T are difference between the βs and V_T of the transistors. In a practical case, $\Delta\beta$ is about 0.2%. Therefore, maximum resolution is about 8 bits if the accuracy is less than half the LSB. Based on Eq. 5.1, the accuracy regarding the mismatch in V_T is given by

$$N = 3.3\log\left(\frac{V_T + \sqrt{2I_{B1}/\beta_c}}{2\sqrt{2}\Delta V_T}\right) - 1 \qquad (5.20)$$

5.8.1.3 Error in Accuracy Due to Offset of Comparator

In the current mode A/D converter, the memory cell performs only the functioning of multiplying the current and the comparator extracts the digital signal from the current information. If the difference between the input current and the reference current is smaller than the offset current of the comparator, the comparator would not able to recognize this difference, and therefore, would not extract the digital signal. Thus, the maximum resolution of the A/D converter is limited by the offset of the comparator. The effect of the offset is compensated for by digital error correction which will be explained in the next section.

5.8.2 Effect of Subtracter Error on the Nonlinearity Error

The effect of subtracter error in the proposed A/D converter is similar to the gain error in a pipelined A/D converter. In a voltage mode converter, errors in the per stage gain have by a variety of sources. In a pipeline using a switched capacitor, these error sources could include capacitor mismatches and non-infinite opamp gains. In current mode, these error sources could include transistor mismatches and nonlinearity of the subtracter gain. An error in the per stage gain causes nonlinearity in the transfer characteristic from input to output of the A/D converter.

The effect of gain error in our proposed current mode A/D converter on the differential nonlinearity (DNL) may be determined graphically as follows. In this analysis, the comparators are assumed to be ideal, reference levels are assumed to be uniform, and the gain is assumed to be linear. Linear gain error is the only nonideality treated in this analy-

sis. Figure 5.18 shows a plot of the amplified residue versus the input for one stage of the analog to digital converter. It is assumed that digital error correction is used to deal with the comparator offset problem. Therefore, this transfer characteristic has twice as many comparator thresholds, and, as a result, the nominal output swing is smaller. The gain error shown produces jumps in the input output transfer characteristic of the A/D converter, which means missing codes.

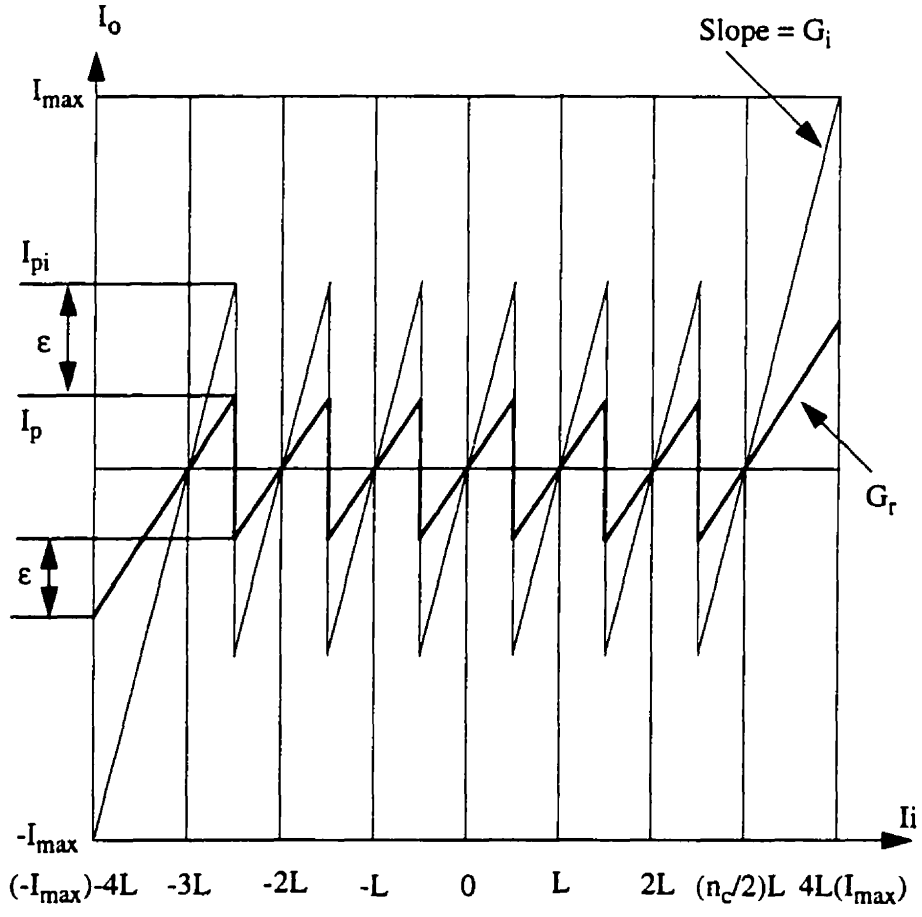

Figure 5.18 The diagram shows the error in the gain of subtracter.

By means of the following analysis, an algebraic relation between the differential nonlinearity (DNL) and the gain error can be determined. It is assumed here that the input range is equal to the output range.

Furthermore, the comparator thresholds are also assumed to be uniform here. The implication of these assumptions of uniform reference levels and comparator thresholds is that the DNL is the same for each transition point. First, the relationship between the reference level L and the number of comparators is determined. L is the reference level subtracted from the input to obtain the residue. From Figure 5.18,

$$I_{max} = G_i\left(I_{max} - \frac{n_c}{2}L\right) \tag{5.21}$$

where n_c is the number of comparator in each stage. I_{max} is the maximum peak swing of the input signal. Because the output swing is assumed to be equal to the input swing in this case, I_{max} is also the peak output swing. By rearranging Eq. 5.21, the following equation is obtained.

$$L = \frac{2}{n_c}\left(1 - \frac{1}{G_i}\right)I_{max} \tag{5.22}$$

L can also be related to the peak value I_p of the residue by the gain:

$$I_{pi} = G_i\frac{L}{2} \qquad I_p = \frac{G_r}{2}L \tag{5.23}$$

The error current at a comparator threshold can be expressed as the difference between I_p and I_{pi} as follows:

$$\varepsilon = I_{pi} - I_p \tag{5.24}$$

Now substitute Eq. 5.22 and Eq. 5.23 into Eq. 5.24 in order to obtain the following expression for the error current as a function of gain error.

$$\varepsilon = \left(\frac{G_i - G_r}{G_i}\right)\left(\frac{G_i - 1}{n_c}\right) I_{max} \tag{5.25}$$

Now, to determine the DNL, note that the amplified residue just to the right of the threshold is too large by ε, while the amplified residue just to the left of the threshold is too small by ε. Therefore, the magnitude of the mismatch between these two points is 2ε. To refer the error back to the input, the error is divided by the ideal gain of the stage with the error and the ideal gain of every stage preceding it. Therefore, the input referred discontinuity in the transfer characteristic of the A/D converter is given as follows:

$$\Delta = \frac{2\varepsilon}{G_i^{k+1}} = \left(\frac{G_i - G_r}{G_i}\right)\left(\frac{G_i - 1}{n_c}\right)\frac{2I_{max}}{G_i^{k+1}} \tag{5.26}$$

The parameter k is the number of gain stages preceding the one with the error. The magnitude of the DNL as a fraction of full scale can then be determined by dividing the input referred value of the discontinuity by the full scale swing of the input. The DNL in LSBs is then found by multiplying by the number of quantization levels in the A/D converter. In the result shown below, N is the number of bits resolved by the A/D Converter.

$$DNL = \frac{\Delta}{2I_{max}} \tag{5.27}$$

The DNL caused by the first stage (k=0) is the largest and is given by the following expression

$$DNL(LSBs) = \left(\frac{G_i - G_r}{G_i}\right)\left(\frac{G_i - 1}{n_c}\right)\frac{2^N}{G_i} \tag{5.28}$$

Note from the above equation that the effect of gain error on DNL can be reduced if the number of comparators is increased. Commonly, A/D converters are built such that $n_c = 2(G_i-1)$. With this assumption and $G_i = 4$ and $(G_i - Gr)/G_i = 1/2^N$, the DNL is 0.125LSB.

5.9 Digital Error Correction

Digital comparator error correction [20], [21] is a technique used to prevent comparator offsets from limiting the resolution of an analog to digital converter. In this technique, the comparator offsets are not corrected. Instead, the A/D converter is designed in a way that is tolerant of comparator offsets. Without digital error correction, the comparator offset must be no more than the least significant bit of the A/D converter. With digital error correction, larger offsets can be tolerated. This technique is attractive because it allows the use of simplified comparators. This can potentially save hardware and power. This technique also allows analog to digital converters to achieve resolutions that would not be possible without it.

To apply this technique to analog to digital converter, extra comparators are added beyond the number that would be needed if the comparators were free of offsets. The full scale linear range of the amplifier must also be extended to accommodate residues that are larger than expected. The following plot of the input output characteristic of one pipeline stage helps to further illustrate how digital error correction works. This plot is useful for deriving a relation between the number of comparators and the maximum allowable comparator offset. Note that in this example the value of the amplified residue is never more than $0.5I_{max}$ in the absence of comparator offsets. If comparator offsets are present, the

amplified residue is still within range, provided that the comparator offset does not go beyond a certain limit.

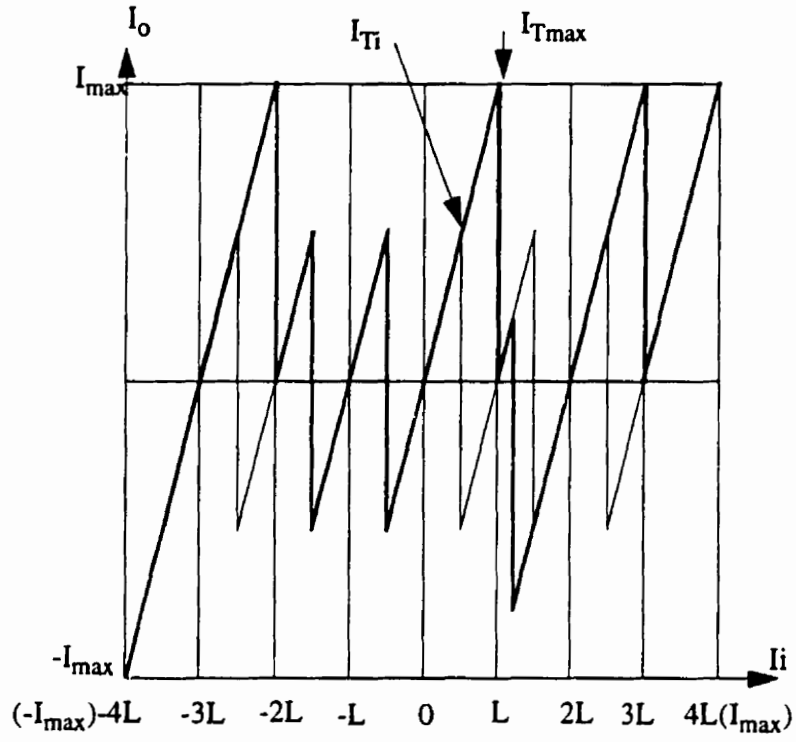

Figure 5.19 Effect of comparator error and its correction.

From Figure 5.18 the following relation can be inferred.

$$GI_{Tmax} = I_{max} \tag{5.29}$$

The maximum allowable comparator offset I_{offmax} at DC is equal to the difference between the maximum comparator threshold given by the above equation and the ideal comparator threshold. For higher input frequencies, the maximum allowable comparator offset is reduced if there is a timing mismatch Δt between the comparator sampling instant and the sample and hold sampling instant.

$$SR \cdot \Delta t + I_{offmax} = I_{Tmax} - I_{Ti} = \frac{I_{max}}{G} - \frac{L}{2} \tag{5.30}$$

where SR is the slew rate of the input signal($2\pi f_{max} I_{max}$). The reference value L in the above equation is given by Eq. 5.22. Substituting for L results in the following formula for the maximum comparator offset.

$$2\pi f_{max} I_{max} \Delta t + I_{offmax} = \frac{I_{max}}{G}\left(1 - \frac{1}{n_c}(G-1)\right) \tag{5.31}$$

From this formula it is evident that the maximum tolerable comparator offset is increased by reducing the interstage gain (residue amplifier gain) and by increasing the number of comparators.

5.10 Simulation and Experimental Results

5.10.1 Test of Nonlinearity Error

The transfer characteristic of an A/D converter is simulated using a code density test with a known waveform at the input. In a code density test, a large number of samples of an input signal are collected and converted to digital codes. Then the number of occurrences of each digital code is plotted on histogram of frequency of occurrence versus code. If enough samples are taken, the effects of noise are averaged out and all the information about the transfer characteristic of the A/D converter can be obtained.

The analysis is based on the transfer characteristic of an A/D converter.By applying a symmetrical signal to the input, each code will repeated for certain period of time. The frequency of each code is proportional to the length of time each code lasts. In general, the number of occurrences N_K of the Kth code is given by

$$\frac{N_K}{N_{total}} = \frac{t(I_{TK+1}) - t(I_{TK})}{t_{total}} \tag{5.32}$$

where I_{TK} is the value of the threshold current and t_{total} is equal to half the period of the input. N_{total} is the total number of samples taken during the code density test, and can be expressed by

$$N_{total} = \sum_{k=0}^{N_{code}-1} N_K \tag{5.33}$$

where N_{code} in the above equation is equal to the number of possible codes output by the A/D converter. By arranging Eq. 5.33, the value of the threshold for the code K with a sine wave input is given by

$$I_{TK} = -\cos\left[\frac{\pi}{N_{total}}\left(\sum_{m=0}^{k} N_m\right)\right] \tag{5.34}$$

The nonlinearity errors can be calculated by using Eq. 5.34. The code density test results presented here were based on samples of a 100KHz sine wave input signal. The resulting DNL and INL are plotted versus the codes in Figure 5.20 and Figure 5.21.

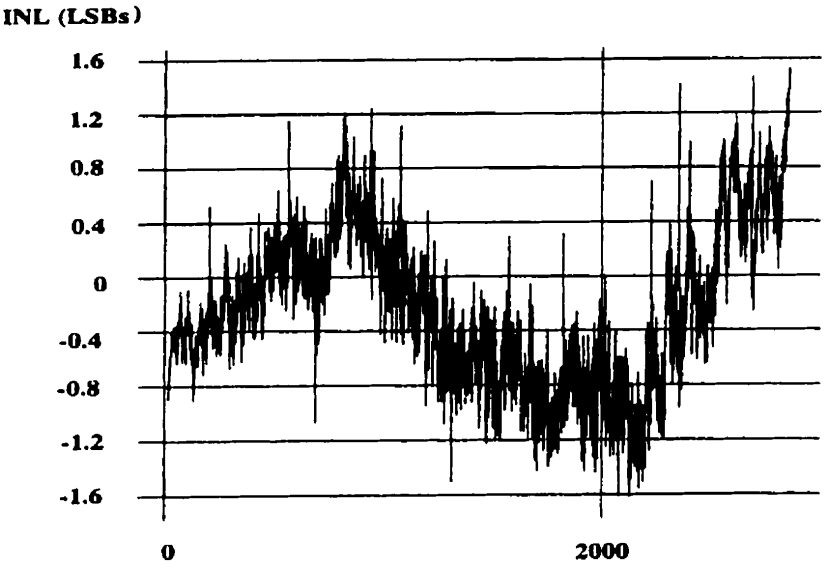

Figure 5.20 Intergral Nonlinearity Versus code in LSBs at 12 bits at input frequency 100KHz.

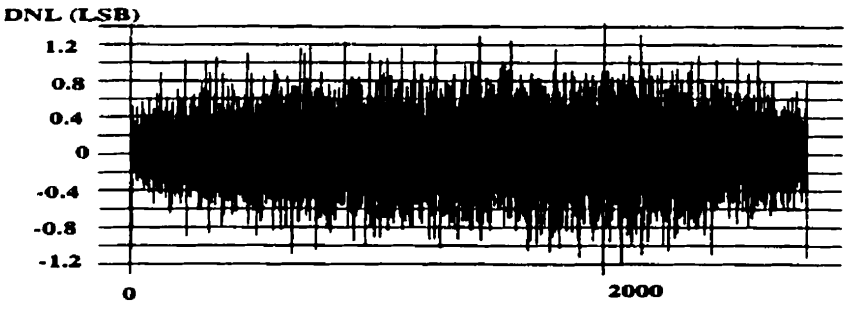

Figure 5.21 DNL error versus code in LSBs in 12-bit A/D converter

5.10.2 Signal To Noise Ratio and Distortion

The signal to noise ratio was calculated by collecting 512 samples of the input signal and performing a 512 point FFT. This test was performed at input frequency of 100KHz. The results of this test are shown in Figure 5.22.

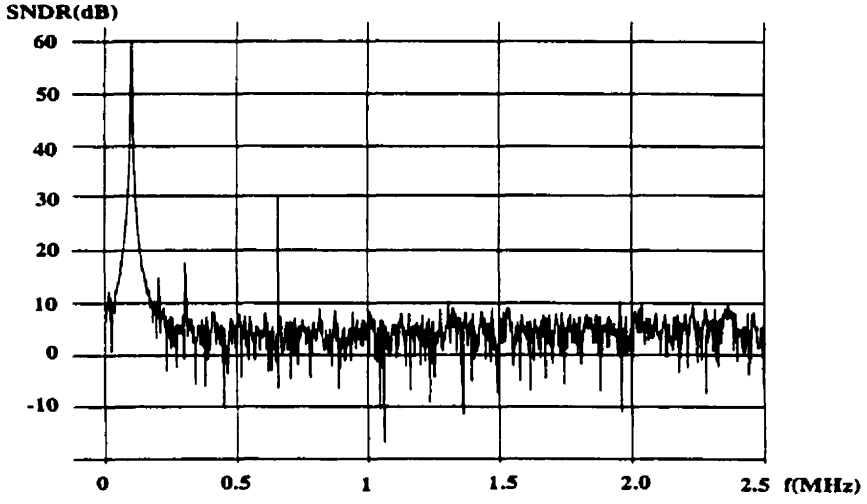

Figure 5.22 Typical 512 point FFT of a 100KHz input sine wave.

5.11 Conclusion

A new architecture for a current mode A/D converter which performs the subtraction and comparison simultaneously is proposed and applied to a 12-bit video-rate A/D converter. The subtraction is performed through a regulated current mirror which uses feedback in order to reduce the mismatch error. A high performance current comparator with a 1 μA offset voltage has been designed to perform the comparison for a 20 MHz analog signal. The circuits are realized with 1.2 μm CMOS MITEL technology.

This A/D converter consists of 6 stages. Each stage consists of six comparators and four subtracters. The speed of conversion has been improved by flash subtracters and by eliminating the S/H between the stages. The SNR is 60 dB, which shows that 10 bits is effective number of bits. Table 5.1 shows the summarized results of this current mode A/D converter.

Table 5.1 The results for the 12-bit A/D converter

Parameters	**Value**
Resolution	12 bits
INL	+,-1.6 LSB
DNL	+,- 1 LSB
SNDR for 100KHz	60 dB
Technology	1.2 um CMOS MITEL
Supply Voltage	+,-1.5 V
Power dissipation	300 mW

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CHAPITRE VI

Un nouveau BIST numérique intégré pour convertisseurs analogique-numérique

6.1 Résumé

La complexité croissante des circuits intégrés analogiques ainsi que l'accès de plus en plus réduit à leurs composants internes, ont rendu la tâche de tester la fonctionnalité de ces composants, un problème majeur durant leur prototypage. Par ailleurs, il y a une forte tendance à intégrer les circuits analogiques avec les circuits numériques sur une même puce où la vérification de la partie analogique est la tâche qui cause le plus de problème.

Dans le chapitre 2, les différents paramètres des convertisseurs A/N ont été discutés. Le grand nombre de paramètres tels que le INL, DNL, le décalage et l'erreur de gain requis pour spécifier complètement les interfaces de conversion de données, et la présence commune des signaux analogiques et numériques dans ces circuits ont rendu la vérification, une tâche plus complexe. De plus, les CAN à haute résolution et à haute vitesse nécessitent des équipements de mesure de haute qualité

Dans ce chapitre, nous présentons une nouvelle approche pour le test de la DNL et de l'INL. Le même test est utilisé pour estimer les erreurs du gain et du décalage. Le test est réalisé dans la partie numérique, ce qui augmente la précision du test. Nous montrerons que ce BIST peut être utilisé pour toute architecture de CAN en ajoutant quelques circuits

additionnels. Nous montrerons également que ce BIST est capable de tester les CAN en pipeline à haute résolution. Dans la première partie, le circuit de base pour le test de DNL et de l'INL est décrit pour un CAN à N bits. Ensuite, nous expliquerons l'application du BIST dans les CAN à approximations successives et les CAN en pipeline. Cette technique est alors appliquée et simulée pour un CAN à 3 bits. Dans la dernière partie, nous exposerons le test d'un CAN en pipeline à 9 bits en recourant à deux techniques différentes. Finalement, nous montrerons que le test du CAN en pipeline peut être accompli en testant uniquement le dernier étage. Notons que l'article proposé dans ce chapitre a été publié dans le "Journal de Microelectronic Reliability, Vol. 38, No. 3, March 1998, pp. 409-420".

A New On Chip Digital BIST For Analog-to-Digital Converter

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This paper has been published in Journal of Microelectronic Reliability, Vol. 38, No. 3, March 1998, pp. 409-420.

6.2 Abstract

A fully digital built-in self-test (BIST) for analog-to-digital converters is presented in this paper. This test circuit is capable of measuring the DNL, INL, offset error and gain error, and mainly consists of several registers and some digital subtracters. The main advantage of this BIST is the ability to test DNL and INL for all codes in the digital domain, which in turn eliminates the necessity of calibration. On the other hand, some parts of the analog-to-digital converter with minor modifications are used in the BIST simultaneously. This also reduces the area overhead and the cost of the test. The proposed BIST structure presents a compromise between test accuracy, area overhead and test cost. The BIST circuitry has been designed using Mitel CMOS 1.5 μm technology. The simulation results of the test show that it can be applied to medium resolution analog-to-digital converter or high resolution pipelined analog-to-digital converter. The presented BIST shows satisfactory results for a 9-bit pipelined analog-to-digital converter.

6.3 Introduction

With the increased complexity of analog VLSI circuits and the reduced access to internal circuits, the task of properly testing these devices is becoming a major bottleneck during their prototyping. In addition there is a strong tendency to integrate analog circuits with digital circuits onto one chip, where the analog testing of the IC is likely to cause most of the test problems.

The analog-to-digital converter(A/D converter) is one of the mixed-signal circuits that has been extensively used for high-speed signal processing applications such as high-performance TV, image recognition, radar, and medical instruments[3]. The large number of parameters required to fully specify the performance of data conversion interfaces and the presence of both analog and digital signal in these circuits make the testing an elaborate task. Furthermore, high speed and high resolution A/D converter require high quality measurement equipment.

Production costs of data converters are dominated by the direct costs of test equipment, test time and the indirect costs of test procedure development[2],[3]. There are two techniques for the testing of data converters. In the first technique, the internal test points of the converter must be available during the test. Although this technique is used extensively, it requires to have stimuli like dc, ac, and noise sources. Furthermore, response evaluation equipment, like dc and ac meters, counters, and waveform analyzers are required. In order to have an efficient controllability and observability, it requires to access much internal nodes. This, in turn, is not practical in most complicated mixed-signal circuits like data converters.

A second completely different approach is to include the stimuli and response evaluation equipment on-chip. From a practical and economical point of view, the variation in

different types of equipment has to be quite limited. Hence, the tests to be carried out and types of faults that can be detected will also be limited. There are, however, a lot of advantages to include Built-In Self Tests(BIST) in data converters[2],[4].

6.4 Previous Works

Analog-to-digital converters are generally nonlinear circuits. There are some important parameters that describe the performance of A/D converters. Some of them describe their static performance and some of them describe their dynamic performance. The static parameters are offset voltage(Off_e), gain error(G_e), differential nonlinearity(DNL) and integral nonlinearlity(INL)[1]. Among them, the accuracy of DNL and INL are critical. This is why DNL and INL are used for fault location and identification of the analog components of a flash A/D converter[5]. Meanwhile, they are used to evaluate the dynamic parameters like signal-to-noise ratio and total harmonic distortion. The performance of any A/D converter depends on these parameters.

The general technique for measuring DNL and INL is based on applying the different analog voltages to the input and checking the transition point by measuring the transition voltages. This is called the servo method. The other technique is the histogram method which involves collecting multiple data points per code step and then calculating INL, DNL and code transition. This technique requires a complicated logic control, an independent input voltage, and a complete analog test circuit. This technique cannot, therefore, be practical for BIST application [12],[13],[14].

Several approaches have been followed and reported in order to have BIST for the test of DNL and INL. The results of some reported designs are based on the fault of specific circuit in A/D converter. On the other hand, the area overhead related to designed BIST based on the specific fault may be comparable to the size of the circuit under the

test. Some of these designs can calculate the DNL in specific and critical codes, which in turn reduces the accuracy of the DNL test. Furthermore, most of the tests in these designs are done in analog domain[2],[6],[10]. Analog area overhead must be tested before testing the A/D converter under test. In most cases, it is not evident to assure completely the functionality of the analog area overhead. In this paper, we attempt to present a fully digital BIST structure for A/D converters having a D/A converter in their structure. It is assumed that, digital area overhead related to BIST structure has been already tested using a BIST structure dedicated to digital part of the chip under test which contains the A/D converter.

In this paper, a new approach for testing DNL and INL is presented. The same test is used for calculating the gain error and the offset error. The test is performed in the digital domain which increases the accuracy of the test. It can be shown that this BIST can be used for any A/D converter architecture having a D/A converter with some additional test circuit. It is also shown that the presented BIST is capable to test high resolution pipelined A/D converter. In the first part, the basic circuit for testing the DNL and INL is described for an N-bit A/D converter. Secondly, the application of BIST in successive approximation and pipelined A/D converterare explained. Then, this technique is applied and simulated for a 3-bit A/D converter. In the last part, the test of 9-bit pipelined A/D converter with two different techniques is explained. It is also shown that the test of a pipelined A/D converter can be performed by testing only the last stage[15].

6.5 Performance Metrics

Nonlinearity parameters generally depend on the ideal input transition voltages and on the real transition voltages. The transition voltage is the analog input voltage in which digital output is changed. The integral nonlinearity is the deviation of the real transition

voltage from the ideal transition voltage after compensation for the gain and offset errors[7],[8],[9]

$$INL(m) = \frac{K_1 V_{rt}(m) - V_{it}(m)}{V_{LSB}} + K_2 \tag{6.1}$$

where $V_{rt}(m)$ and $V_{it}(m)$ are the analog transition voltages in the real and ideal cases for code m, $n = 2^N$, and N is the number of bits. K_1 and K_2 are constants such that INL(1) = INL(n) = 0.

The differential nonlinearity, DNL, of an A/D converter is obtained by a first order difference of the integral nonlinearity, INL. The DNL error excluding offset and gain errors is given by Eq. 6.2.

$$DNL(m) = \frac{V_{rt}(m+1) - V_{rt}(m)}{V_{LSB}} - 1LSB \tag{6.2}$$

The DNL error can be found by INL:

$$DNL(m) = INL(m+1) - INL(m) \tag{6.3}$$

INL in Eq. 6.3 is used from Eq. 6.1 which is free of gain and offset errors.

On the other hand, the offset error and gain error can be obtained by INL in the first code and in the last code. Therefore:

$$V_{offe} = \frac{V_{rt}(1) - V_{it}(1)}{V_{LSB}} = INL(1) \tag{6.4}$$

$$G_{err} = INL(n) - INL(1) \tag{6.5}$$

These equations show that the information about the transition voltage in the ideal and real cases are required for calculating the static parameters. Eq. 3 also shows that it is possible to obtain the DNL from INL results. The maximum acceptable error for DNL and INL is $\pm 1/2$ LSB.

6.6 BIST Architecture for Static A/D converter Testing

Test accuracy and area overhead are the most essential performance of analog and mixed-signal BIST schemes. Most of the BISTs for testing A/D converter require a digital-to-analog converter(D/A converter) in their structures. The resolution of required D/A converter should be at least one bit more than the resolution of an A/D converter under test. In order to reduce the area overhead, the proposed BIST approach doesn't use an extra D/A converter, as proposed in previous works[11]. In our digital BIST, we are using the same D/A converter which is used in the architecture of an A/D converter, except that its resolution is increased during the test. Meanwhile, the accuracy of test is increased because the test is done in the digital domain.

6.6.1 A Digital BIST for A/D converter Testing

The new technique is based on the relative error in the digital output. With this technique, the transition voltage is generated by a counter. A digital circuit compares the A/D converter output with the previous one. The transition voltage can be used if the result of the comparison is positive. Therefore, this voltage is used instead of the ideal transition voltage in the INL test. This voltage is also used as a new transition voltage for the DNL test. The main benefit of this technique is to test INL and DNL in all A/D converter codes, which in turn increases the accuracy of the test. It is also possible to test DNL using INL information.

Figure 6.1 shows a digital BIST as a block. The inputs of this block are digital data of A/D converter, clock, and test signal control. The outputs of this BIST circuit are INL_{max}, DNL_{max}, Off_e, G_e, and the sign of DNL and INL, S_D and S_I respectively.

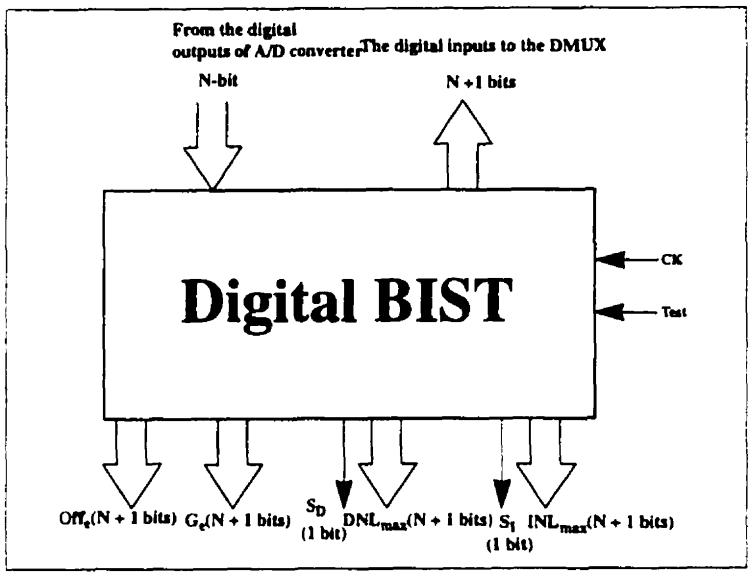


Figure 6.1 Digital BIST with its inputs and outputs

Figure 6.2 shows the complete architecture of the digital BIST circuit for measurement and testing the static parameters of A/D converter. The test architecture mainly consists of the following six parts:

- An (N+1)-bit counter which generates the input test vector.
- Control logic unit which generates proportional control signals for the test circuit.
- Two N-bits registers and some (N+1)-bit registers in order to save output data in different parts of the digital circuit.
- Two full subtracters and one full adder for calculating the DNL and INL
- Three combinational logic circuits which operate as 3 digital comparators.

- The interface circuits between the digital BIST circuit and A/D converter under test consists of a digital multiplexer(DMUX) and some switches.

Figure 6.3 shows the flow chart for testing of INL and DNL. In the beginning, all the registers are reset. The main analog input of the A/D converter is disconnected. In the next step, the A/D converter is transferred to the test mode. In this step, the resolution of the D/A converter is increased by one. Its inputs are connected to the counter. The output of the counter is saved in register R_R. The outputs of D/A converter are connected to the input of A/D converter and saved in the sample and hold circuit. Then, the A/D converter is rearranged to its functional mode and converts the saved voltage in the sample and hold circuit. The digital output of the A/D converter is saved in register R_B.

The transition voltage should be tested whenever a digital code is available in the output. This can be done by comparing register R_A with register R_B in a digital comparator. There is a transition if the digital output T is "1".

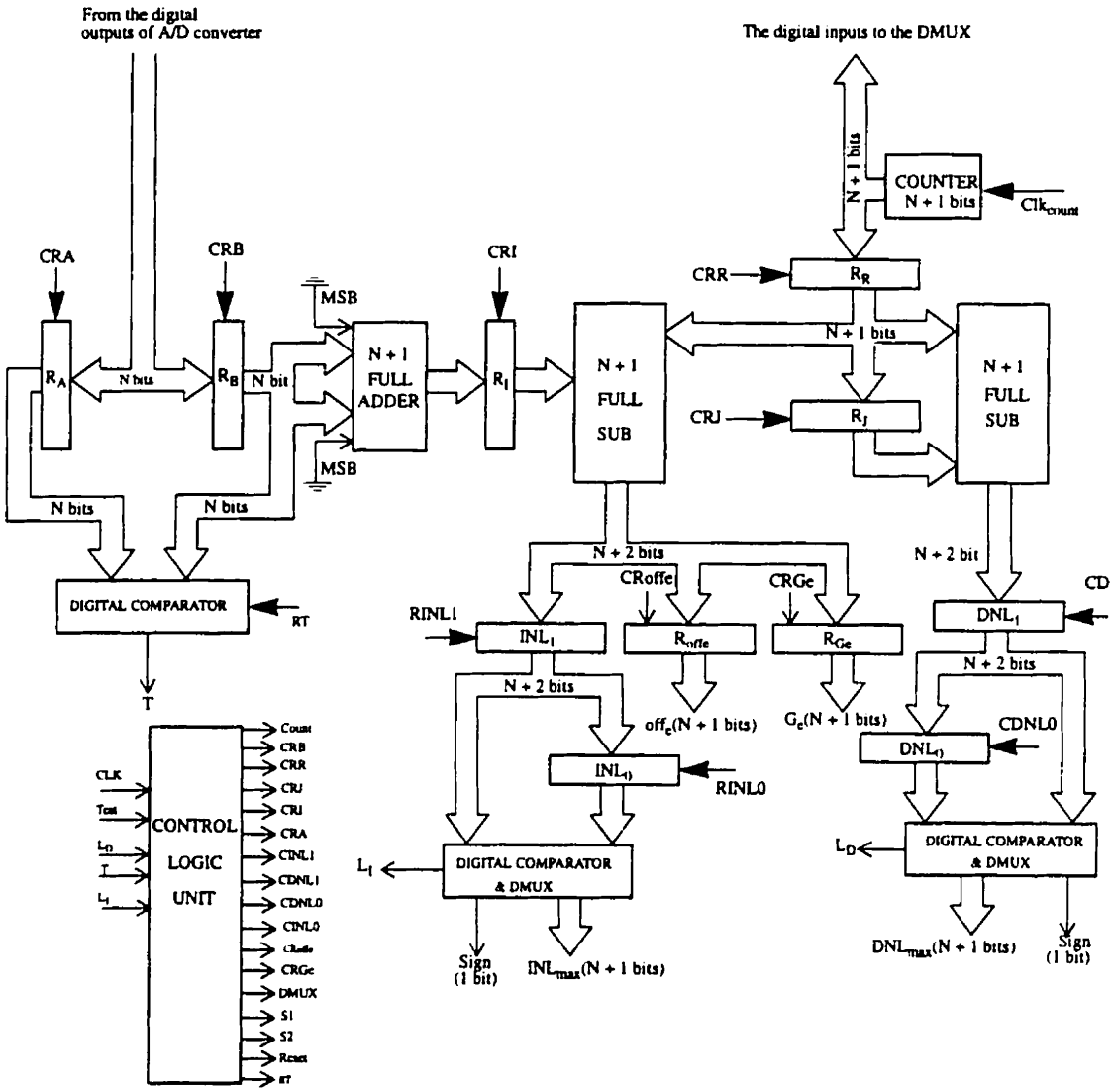


Figure 6.2 The architecture of the proposed digital BIST

The next step of the flow chart depends on the digital output T. If the digital output T is "0", the counter should be incremented by one and the test continued. If the digital control T is "1", the digital output of the A/D converter should be converted from N bits to N+1 bits. In this BIST, the reference voltage is the same reference voltage as in A/D con-

verter, meaning that the LSB in the N-bits A/D converter is twice the LSB in the (N+1)-bit A/D converter. Therefore, the conversion can be done by using a (N+1)-bit full adder in which both input bits are connected to the same register R_B. The two most significant bits(MSB) inputs are connected to ground. The output of the full adder is then saved in register R_I.

6.6.2 INL Testing

The next step is the INL calculation. The ideal transition is in register R_I and the real transition is in register R_R. Therefore, the INL is the difference between the digital code in R_R and R_I. The result of this subtraction is given by N+1 bits. This means that the unit of the INL is 1/2 LSB of an N bits A/D converter.

$$INL = R_R - R_I \tag{6.6}$$

INL_{max} can be found by comparing the digital codes in register INL_I with INL_0. Finally, INL_{max} is in the register INL_0.

6.6.3 DNL Testing

The calculation step for the DNL is the same as INL calculation step. The real transition voltage in the previous code was saved in register R_J. Therefore, the digital code in registers R_R and R_J should be subtracted in order to find the DNL

$$DNL = R_R - R_J \tag{6.7}$$

DNL_{max} can be found by comparing the digital codes in register DNL_I with DNL_0. Finally, DNL_{max} is in the registers DNL_0.

At the end, the digital codes in registers R_B and R_R are transferred to registers R_A and R_J, respectively.

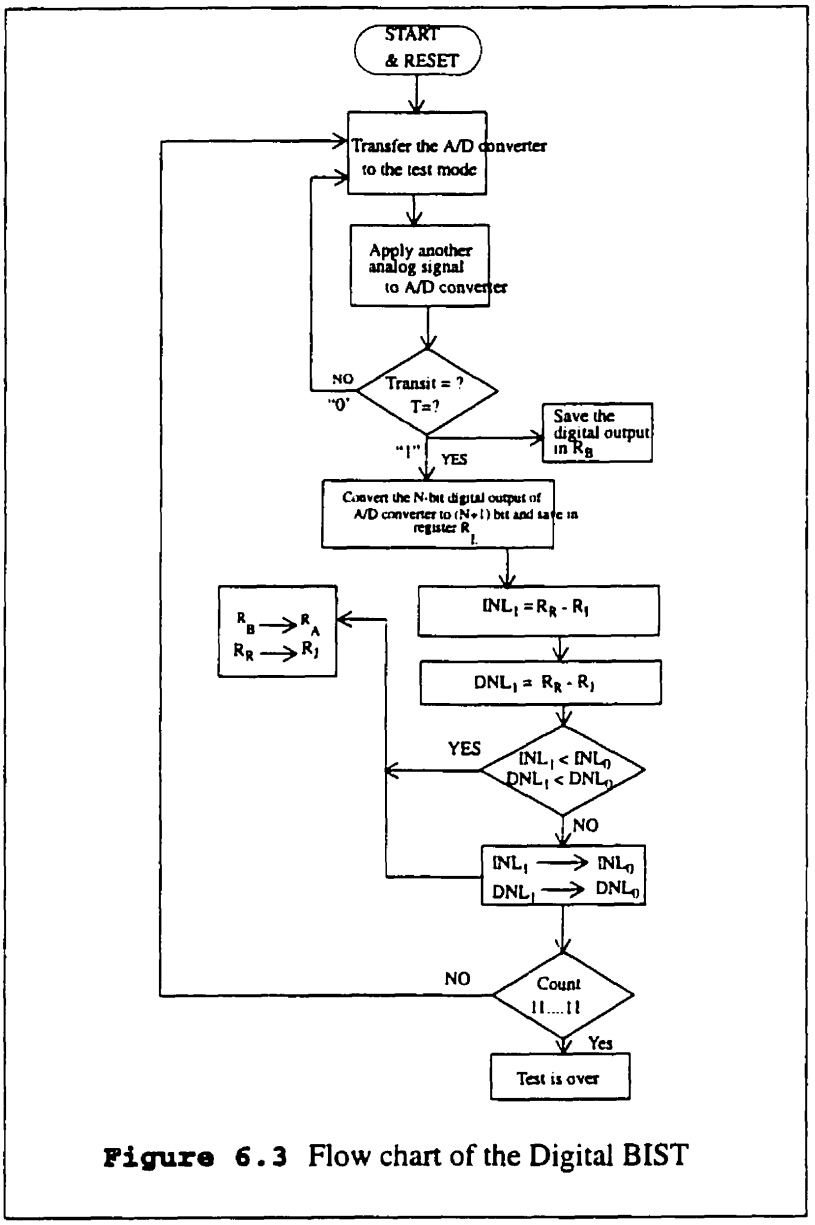


Figure 6.3 Flow chart of the Digital BIST

6.6.4 Offset and Gain Error Testing

The offset error is the INL in the first code. This error is saved in register R_{offe}. The offset error should be compensated during the DNL and INL test. The gain error is the

INL in the last code. This error is saved in register R_{Ge}. The clock of registers R_{offe} and R_{Ge} are only active in the first code and last code, respectively.

6.7 BIST for Successive Approximation A/D converter

Successive approximation is a technique which is extensively used for low speed and high resolution converters. It consists of a comparator, a D/A converter, decision logic, and decision registers. The presented BIST can be used for the test of this converter, as shown in Figure 6.4. In order to use the same D/A converter for the BIST, it is required to increase its resolution by one during the test mode. In the normal mode of operation, the MSB input of D/A converter is grounded. Therefore, it operates as a N-bit D/A converter.

The digital BIST is connected to A/D converter by two digital multiplexer. The first one is multiplexing between the output of the counter, which come from the BIST, and the outputs of the decision registers. The second one is multiplexing between ground and the MSB output of the first multiplexer. The N-bit outputs of the first multiplexer are con-

nected to the N-bit inputs of D/A converter. The output of the second multiplexer is connected to the MSB input of the D/A converter.

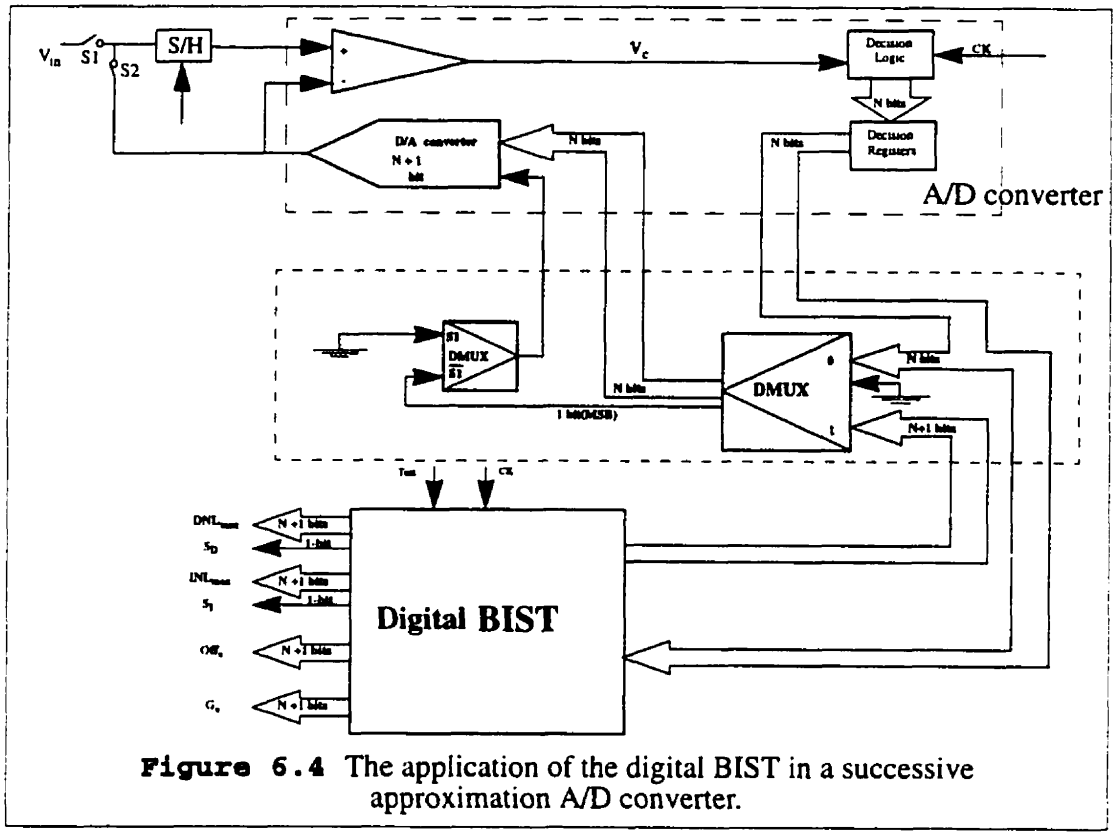


Figure 6.4 The application of the digital BIST in a successive approximation A/D converter.

The inputs of the comparator in Figure 6.4 will be selected by two switches S1 and S2 depending on their states. Figure 6.5 shows the timing diagram of the test. The test starts by turning S1 off and reset all the registers at "t1". In this mood, the A/D converter is disconnected from its external inputs and will be transferred to the test mode. In the next step,"t2", the S2 turns on and the first mux connects the output of the counter to the inputs of D/A converter. The output voltage of the D/A is then saved in the S/H circuit and S2 turns off, "t3". The D/A returns to its original resolution and the A/D converter converts the saved voltage in the S/H circuits. The register R_R in the BIST will save the counter output as the real transition in DNL test and ideal transition in INL test. Now, the A/D

converter starts its normal operation. The digital code of A/D converter will be ready at "t4". At this time, the digital BIST starts its operation on this code. At "t5", the BIST will continue for the test of the next code. The R_{offe} will be active only in the first INL test. The R_{Ge} will be active only in the last INL test.

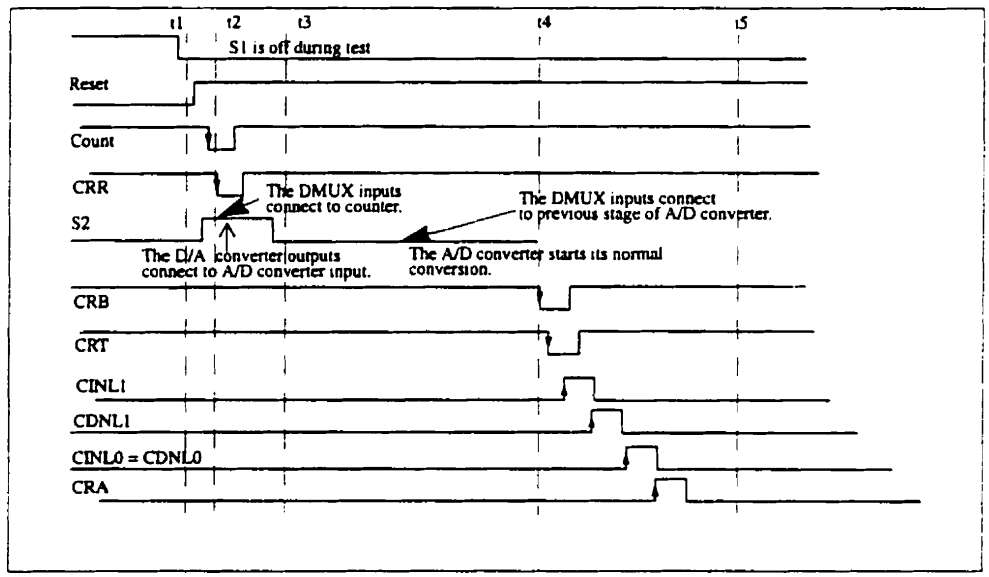


Figure 6.5 The clock diagram of the digital BIST

The DNL and INL testing procedure takes 6 clock cycles for each code. Therefore, the complete testing time is

$$T_{total} = \frac{6 \times 2^N}{f} \tag{6.8}$$

where f is the clock frequency of the BIST. The clock of BIST is limited by the settling time of the D/A converter and conversion time of the A/D converter.

6.8 Application of BIST in Pipelined A/D converter

Here, we show how the presented BIST can be integrated for the test of a pipelined A/D converter. In this method, the BIST is required only for the last stage. The INL and DNL from the last stage is used to calculate the INL and DNL in a complete A/D converter. The following equations show how we can utilize the digital BIST for testing a pipelined A/D converter. In the first step, some parameters are defined regarding to the pipelined architecture:

- $[k_{jp}]$: the decimal code of a digital code j in stage p where $[k_{jp}]$ can be $0,\ldots,(2^n - 1)$.
- m: the number of stage
- n: the resolution of each stage
- V_{ref}: the reference voltage in all stages
- LSB: the least significant bit of each stage
- $V_{it}([k_{jp}])$: the ideal transition voltage for code j in stage p normalized by LSB
- $V_{rt}([k_{jp}])$: the real transition voltage for code j in stage p normalized by LSB
- lsb: the least significant bit of N=mn bits A/D converter

The real transition voltage of code j in stage l is given by:

$$V_{rt}([k_{jl}]) = V_{it}([k_{jl}]) + \Delta_{k_{jl}} \tag{6.9}$$

where $\Delta_{k_{jl}}$ is normalized deviation of real transition voltage from ideal transition voltage. Therefore the INL in this code is given by:

$$INL[k_{jl}] = V_{rt}([k_{jl}]) - V_{it}([k_{jl}]) = \Delta_{k_{jl}} \tag{6.10}$$

where $V_{it}([k_{jl}])$is given by:

$$V_{it}([k_{j1}]) = \frac{[k_{j1}]V_{ref}}{2^n} = [k_{j1}]LSB \tag{6.11}$$

The real transition voltage in a 3 stage pipelined with similar stages is given by:

$$V_{rt}[k_{j1}k_{l2}k_{q3}] = \frac{\Delta_{k_{q3}}}{2^{2n}} + \left(\frac{[k_{q3}]}{2^{2n}} + \frac{[k_{l2}]}{2^n} + [k_{j1}]\right)LSB \tag{6.12}$$

Therefore, the INL for this pipelined A/D converter can be found from Eq. 6.7:

$$INL[k_{j1}k_{l2}k_{q3}] = \frac{\Delta_{k_{q3}}}{2^{2n}} = \frac{INL[k_{q3}]}{2^{2n}} \tag{6.13}$$

This equation can be extended for m stage pipelined A/D converter as follows:

$$INL[k_{j1}k_{l2}\ldots k_{qm}] = \frac{INL[k_{qm}]}{2^{(m-1)n}} \tag{6.14}$$

The DNL in each code can be found from Eq.3 and Eq.9:

$$DNL[k_{j1}k_{l2}\ldots k_{qm}] = \frac{DNL[k_{qm}]}{2^{(m-1)n}} \tag{6.15}$$

These equations show that the pipelined A/D converter can be tested only by testing the last stage if all stages have similar source errors. Eq. 6.14 and Eq. 6.15 are valid when there is no missed code in any stage before the last stage.

For example, in a pipelined A/D converter, n, m, and N are 2, 3, and 6 respectively. If the INL in decimal code 2[10] of the last stage is 0.25LSB, then the INL in digital code 38[100110] will be -0.015625LSB or 0.25lsb.

Figure 6.6 shows the application of the digital BIST in order to test a 9-bit pipelined A/D converter. In this test method, the digital BIST is used to test only the last stage. Then, the results of test are used in Eq. 6.14 and Eq. 6.15 to compute DNL and INL errors of a 9-bit pipelined A/D converter . Figure 6.11b and Figure 6.12b, illustrate the computed test results for DNL and INL, respectively. Figure 6.6 also shows that the interface circuits between digital BIST and one stage of pipelined A/D converter are the same as that described in the successive approximation method.

Note, however, that we can apply the digital BIST for a complete test of 9-bit pipelined A/D converter as a *black box*, shown in Figure 6.7. Here, the digital BIST has to use an external 10-bit D/A converter. Figure 6.11a and Figure 6.12a show the results of DNL and INL when a pipelined A/D converter is tested as a *black box* by the digital BIST.

Comparing the results of the stage test approach and the *complete* test approach shows that stage testing is an accurate and economic test technique for pipelined A/D converter.

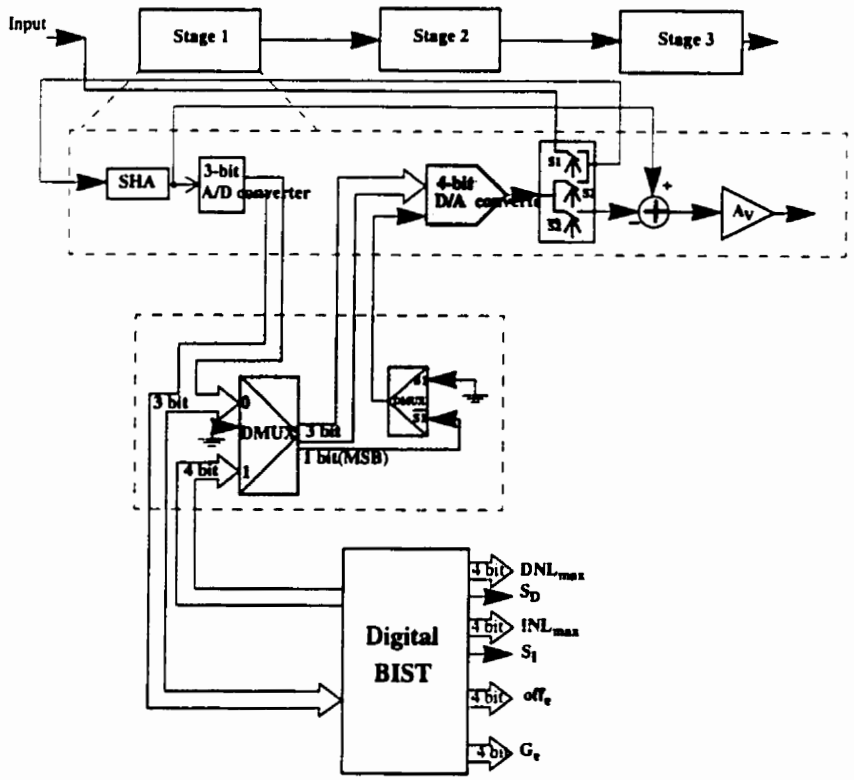


Figure 6.6 The digital BIST used for the test of one stage of 9-bit pipelined A/D converter.

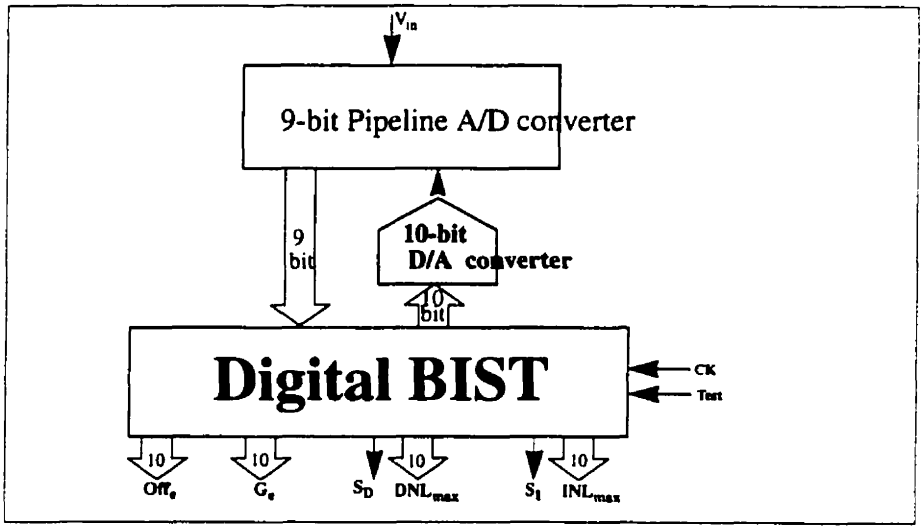


Figure 6.7 The application of the digital BIST in 9-bit pipelined analog-to-digital converter

6.9 Simulation and Experimental Results

The test circuit has been designed for a 3-bit flash A/D converter in 1.5 μm Mitel CMOS technology. This unit cell is then utilized to test a pipelined A/D converter. Table 6.1 shows the ideal, experimental, and simulation transition voltages. The ideal and experimental characteristics of this A/D converter are shown in Figure 6.8. Figure 6.9 shows the DNL simulation results with its sign. The DNL is about 1*LSB* which is comparable with the experimental result. Figure 6.10 shows the INL test with its sign. The INL is about -1.5*LSB*. The outputs in Figure 6.9 and Figure 6.10 are 4 bits meaning that the unit is 1/2 LSB. The sign is only one bit which is "1" for negative and is "0" for positive.

The presented BIST is used to test a 9-bit pipelined A/D converter. Each stage has 3-bit resolution. The pipelined A/D converter uses the same faulty 3-bit A/D converter. The BIST is employed to test the 9-bit A/D converter by two different approaches. In the first approach, the last stage is tested. This test is done by 4-bit digital BIST as shown in Figure

6.6. The result of the last stage is applied to the equations in order to compute the INL and DNL in all A/D converter codes. In the second approach, the complete 9-bit pipelined A/D converter is tested by 10-bit digital BIST as shown in Figure 6.7. Figures 11a, 11b, 12a and 12b show the DNL and INL results for 9-bit A/D converter in the two different test approaches. The figures show that INL and DNL for 9-bit pipelined A/D converter is -1.5*lsb* and 1*lsb* respectively. Figure 11 shows that the DNL results in stage testing and complete testing have 10% difference. Figure 12 shows the same difference for INL results.

The area of the designed BIST circuits for 9-bit pipelined A/D converter is about 2.5 mm^2. Base on the average of medium to high resolution A/D converter[17],[18],[19],[20],[21],[22],[23], the area overhead is 20% of the total A/D converter's chip area. The total test time has been reduced to $6 \times 2^N \times T$, which is

Table 6.1 Results of transition voltage in 3-bit A/D converter

Code	ideal (LSB)	Experimental (LSB)	Simulation (LSB)
000	0	0	0
001	1	0.9	1
010	2	missed	missed
011	3	1.4	1.5
100	4	3.2	3.5
101	5	4	4
110	6	5.7	6
111	7	6.1	6.5

significantly shorter than that spent when using external test equipment.

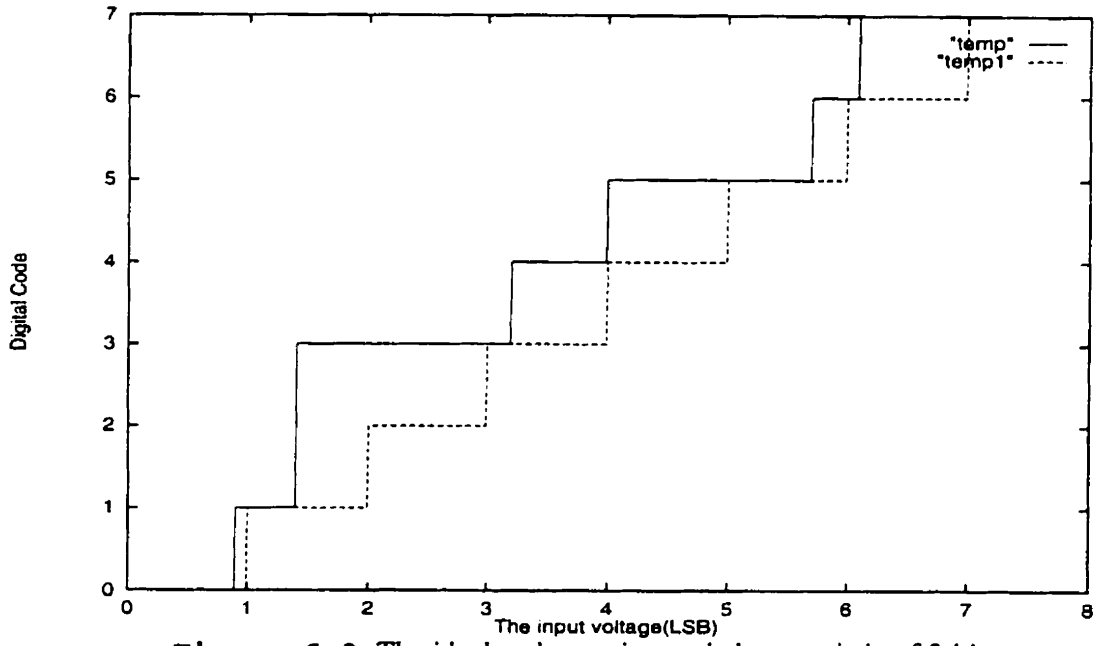


Figure 6.8 The ideal and experimental characteristic of 3-bit A/D converter

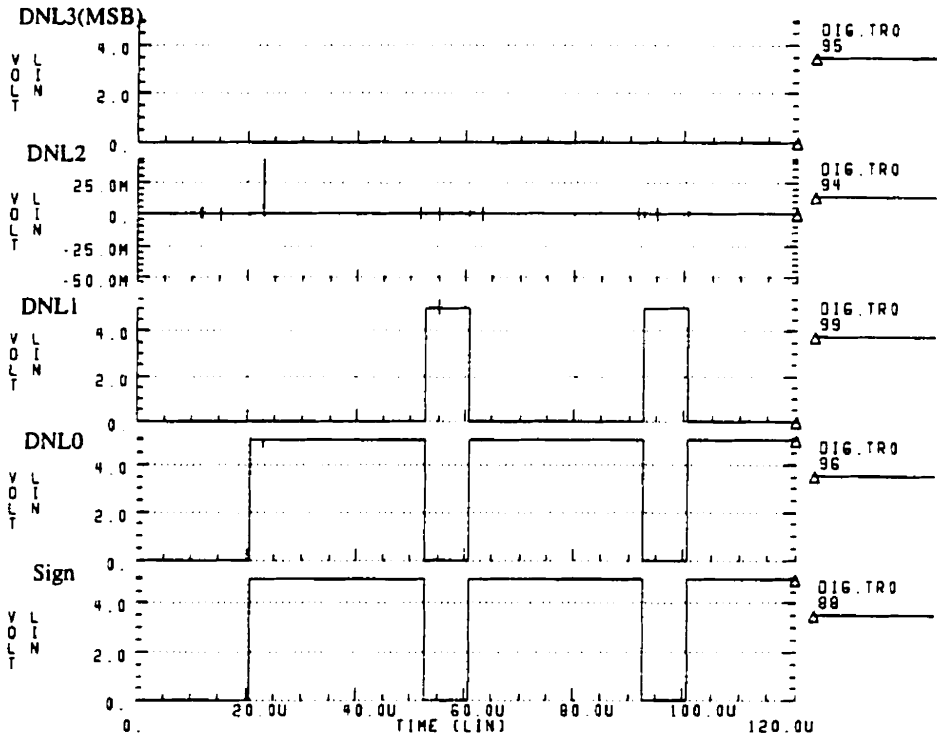


Figure 6.9 The simulation results for DNL test in 3-bit A/D converter using digital BIST.

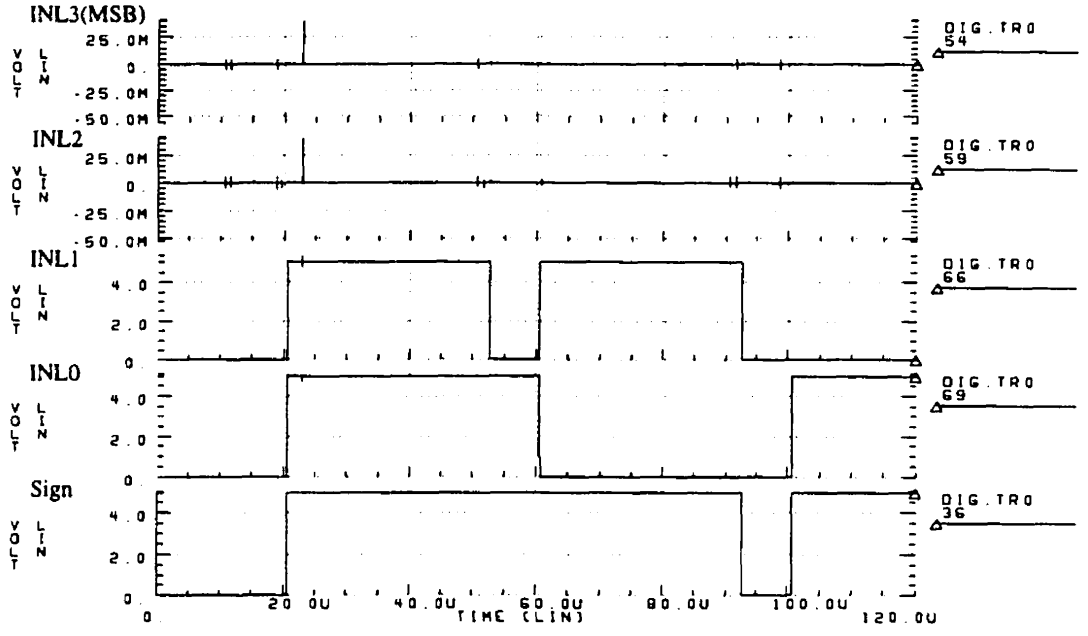


Figure 6.10 The simulation results for INL test in 3-bit A/D converter.

6.10 Conclusion and Discussion

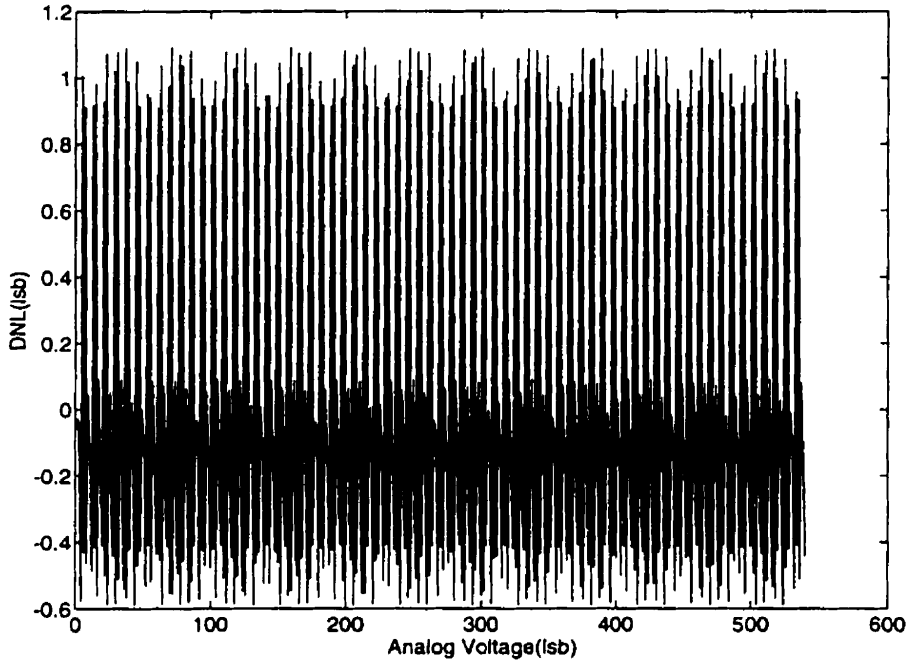
The complete BIST circuit has been designed for testing the INL, DNL, gain error, and offset error of an analog-to-digital converter. The test is done in the digital domain which eliminates the necessity of calibration. The simulation shows satisfactory results for a 3-bit flash A/D converter and a 9-bit pipelined A/D converter. The main circuit used in the BIST circuit is a D/A converter which can be found in the majority of A/D converters. The only difference is that the D/A converter, in this BIST design, can perform two tasks: a first task related to A/D converter architecture and the second one as described in the proposed BIST scheme. When the A/D converter is in normal operation, the resolution of the D/A converter is N bits. On the other hand, the resolution of the D/A converter is (N+2) bits during the test mood. The accuracy of the test can be increased by increasing the resolution of the D/A converter and the counter.

The presented BIST is very useful for high resolution pipelined A/D converters. This is because we can test a pipelined A/D converter by testing the last stage. It has been shown that the BIST can employ the same D/A converter as in pipelined. Therefore, this BIST can give a good fault coverage in high resolution pipelined A/D converters. Hence, the area overhead, test time, and accuracy will be improved significantly.

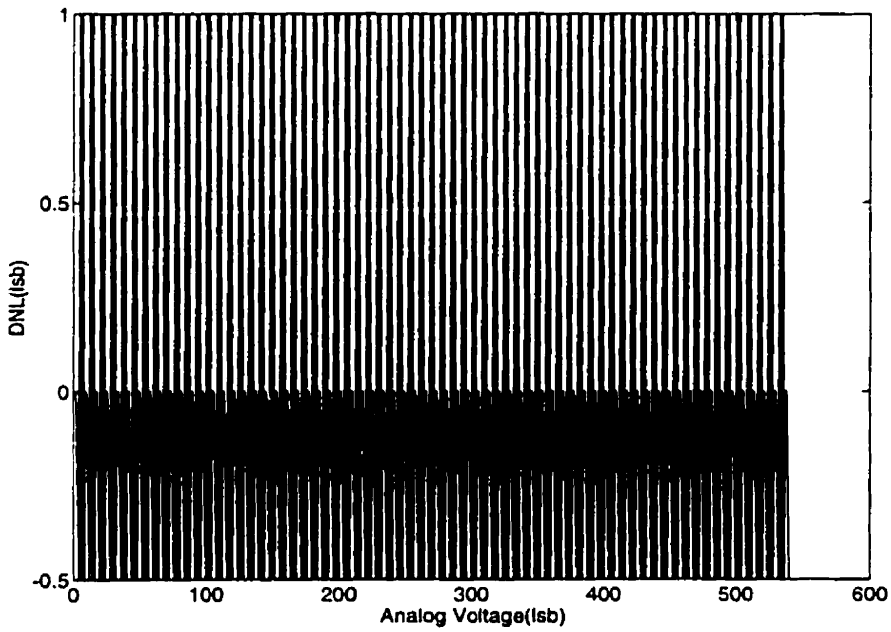
BIST techniques which operates in the analog domain, require some additional circuits for its calibration[2]. The presented BIST operates in the digital domain. Therefore, there is no need for calibration circuits.

Area overhead related to BIST structure is tested using BIST architecture of the chip under test. In addition, in the majority of applications A/D converters are embedded in an ASIC which consists of a microcontroller or a versatile control logic. In this case, all digital operations can be performed using the embedded microcontroller which decreases the area overhead related to the BIST structure.

Normally, the main error sources in any A/D converter are related to comparators, amplifiers, switches, reference voltages, and D/A converter. This digital BIST is not based on the fault of a specific circuit in A/D converter. Hence, the digital BIST can cover all functional faults. During the test mood, the D/A converter also performs two tasks. When D/A converter circuit is connected to the counter in the BIST, it is assumed to be fault-free. In the conversion and test mood, the same D/A converter is used for conversion. In this case, it is assumed to be faulty. Therefore, there can be some errors on the test results based on the first assumption. These errors can be detected by using an analog high performance BIST for D/A converter[2]. The integration of the presented digital BIST with analog BIST for D/A converter in [2] can give a high performance mixed-signal BIST for high resolution and high speed A/D converters.

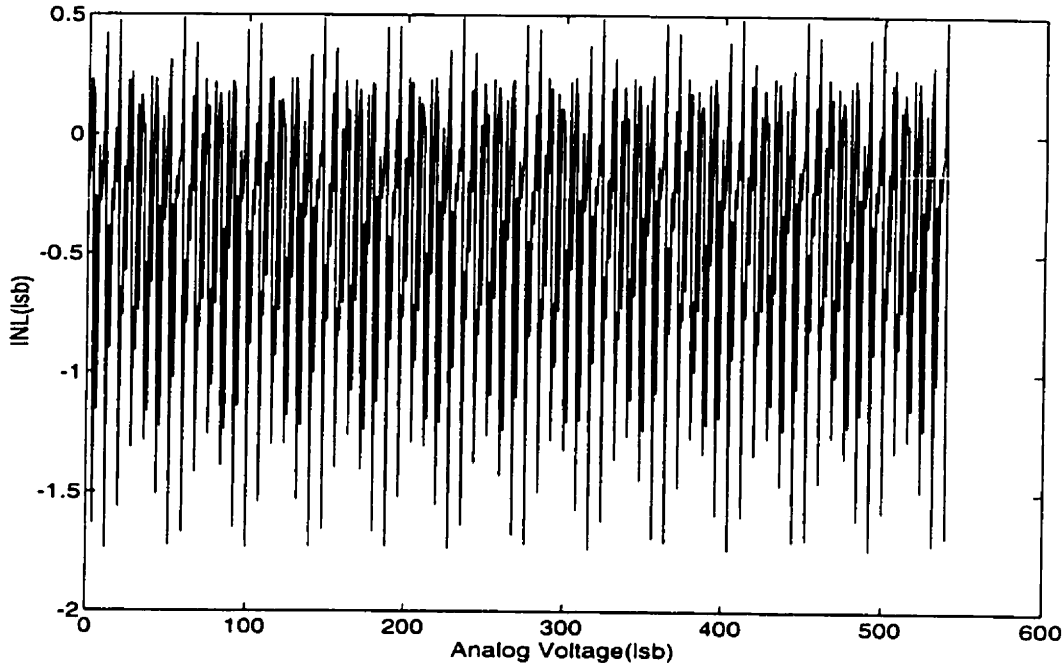


(a)

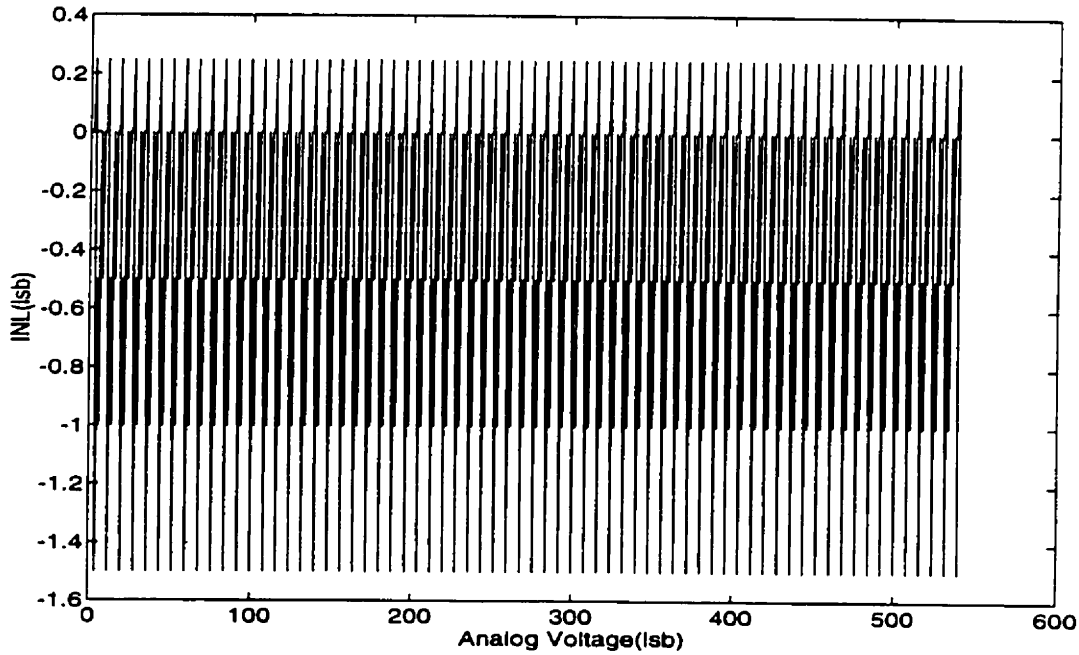


(b)

Figure 6.11 DNL nonlinearity for 9-bit pipelined A/D converter : a) Complete test b) Stage test.



(a)



(b)

Figure 6.12 INL nonlinearity for 9-bit pipelined A/D converter: a) Complete test b) Satge test.

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CHAPITRE VII

Conclusion

7.1 Conclusion et Remarques

Depuis plusieurs années, le rôle traditionnel des circuits analogiques a changé d'un processeur de signal à une interface entre un DSP et le monde extérieur qui est en général analogique. Par conséquent, le nouveau rôle des circuits analogiques est d'acquérir toutes les caractéristiques nécessaires pour co-exister avec l'environnement numérique qui est dominant. La performance des circuits analogiques doit correspondre avec celles des circuits numériques. En plus, les circuits analogiques doivent être implantés en utilisant un procédé de fabrication qui est utilisé pour les circuits numériques. De cette manière, le convertisseur analogique/numérique joue un rôle important comme une interface entre la partie numérique et la partie analogique.

Une nouvelle architecture a été explorée dans le but d'avoir un convertisseur analogique/numérique de grande performance. Les techniques utilisées pour atteindre les objectifs de notre recherche sont classifiées en trois niveau; l'architecture, le circuit et le test. Concernant l'architecture, le choix de faire la comparaison et la soustraction en parallèle par étage permet de compenser le délai dû à la soustraction et au convertisseur numérique-analogique N/A. Ceci a pour effet d'enlever le convertisseur N/A d'une architecture conventionnelle.

Au niveau circuit, la contribution consiste en deux parties: la conception et l'investigation du convertisseur A/N proposé en mode tension et en mode courant. Pour concevoir

le convertisseur A/N en mode tension, les sous-circuits doivent être conçus soigneusement. Les sous-circuits consistent en un soustracteur et un comparateur. Par conséquent, la première contribution en mode tension, est la conception d'un amplificateur opérationnel de haute performance, qui nous aide à réaliser un soustracteur ayant le minimum d'erreur et de retard. Pour cela, un amplificateur opérationnel très rapide, ayant un pré-amplificateur et un étage cascode sont utilisés pour obtenir une bande passante très élevée. En plus, la technique de compensation "feedforward" a été utilisée pour la réduction du temps de stabilisation. Les résultats expérimentaux obtenus sont 90 dB comme gain en mode DC et 4 ns pour le temps de stabilisation, ce qui est meilleur que les résultats des circuits publiés en technologie BiCMOS. La seconde contribution dans le circuit en mode tension est la conception d'un comparateur à faible consommation et à faible décalage et cela en profitant de la correction des erreurs. Ces sous-circuits ont été ensuite utilisés pour vérifier le convertisseur A/N proposé en mode tension.

Pour vérifier le comportement du convertisseur analogique/numérique (A/N) en mode tension, nous avons conçu un convertisseur de 3 bits en utilisant une technologie BiCMOS de 0.8 μm. Ce convertisseur, suivi d'un convertisseur flash standard de 8 bits permet une conversion de 11 bits. Le convertisseur analogique/numérique fonctionne à 1 MHz avec un rapport signal sur bruit de 62 dB. Nous avons trouvé que les erreurs de non-linéarité INL et DNL sont inférieurs à 1 LSB pour un convertisseur A/N de 11 bits.

La conception du convertisseur A/N en utilisant le mode courant est une autre contribution au niveau circuit de cette thèse. Après la vérification des performances de l'architecture proposée en mode tension, il est nécessaire d'améliorer ses performances en tenant compte des avantages des circuits en mode courant comme la vitesse et l'alimentation à faible tension. Les avantages des circuits en mode courant consistent en la possibilité de

faire correspondre les performances et le procédé technologique des circuits analogiques à celle des circuits numériques, en réduisant l'utilisation des condensateurs linéaires et en utilisant une faible tension d'alimentation. Pour les circuits à échelle d'intégration réduite, le fait de réduire la tension d'alimentation ne va pas de réduire le rang dynamique et le rapport signal sur bruit. Cependant, les caractéristiques non-idéales des transistors MOS affectent d'une manière significative la performance des circuits en mode courant, et rendent l'utilisation des circuits en mode courant moins bénéfiques, en la comparant aux circuits analogiques utilisant les capacités commutées. Par conséquent, cette contribution consiste en deux parties. La première est de concevoir un commutateur en mode courant à haute performance pour réduire quelques effets de non-idéalités des transistors MOS. La deuxième est de modifier l'architecture proposée du convertisseur A/N en utilisant des commutateurs en mode courant et, par la suite, obtenir un convertisseur A/N à haute performance et avec une faible tension d'alimentation.

Pour réduire l'effet des caractéristiques non-idéales des transistors MOS, un commutateur en mode courant de haute performance a été développé. Ce commutateur utilise un circuit à cascade de régulation. Les effets non-idéaux aux transistors MOS ont été analysés. L'analyse théorique et les simulations montrent que le commutateur proposé a une meilleure performance que les commutateurs existant basés sur la transmission de courant d'opération. Le temps de stabilisation des commutateurs et la mémoire de courant ont été aussi étudiés. Deux circuits prototypes ont été conçus et fabriqués. Les deux circuits ont été implantés en utilisant un procédé de fabrication de MITEL CMOS de 1.2 µm. Les performances du commutateur de courant ont été évaluées en terme d'erreurs de gain, perte par insertion, isolation et temps de stabilisation. Les résultats des tests ont montré que les cellules ont une petite erreur de gain, une petite perte de puissance, et sont capables d'opé-

rer avec une tension d'alimentation dont l'intervalle est de 3 et 5 volts. Ces commutateurs ont été utilisés dans les convertisseurs analogique/numérique en mode courant.

La deuxième partie de la contribution portant sur l'architecture en mode courant est de développer le convertisseur A/N proposé. L'architecture du convertisseur A/N a été modifiée en utilisant une matrice de commutateurs en mode courant. Un prototype a été développé avec un procédé de fabrication CMOS de MITEL de 1.2 µm. Les résultats de simulation et les résultats expérimentaux sont présentés dans les chapitres 4 et 5. À une vitesse de conversion de 40MS/s, le convertisseur A/N a un SNDR maximum de 60 dB avec une fréquence d'entrée de 100kHz. Les courbes de DNL et du INL montrent une bonne correspondance des résultats SNDR.

Le convertisseur A/N a été conçu pour une résolution de 12 bits. L'erreur de décalage des comparateurs de courant a été réduite avec la méthode de correction numérique. Cependant, les autres types d'erreurs limitent la marge dynamique de ce convertisseur à 11 bits.

Dans le but de comparer le convertisseur A/N proposé avec les architectures les plus récentes mentionnées dans le Chapitre 2, la figure de mérite (FOM) est défini comme suit:

$$FOM = \frac{f_s \cdot SNR}{P_{dis} \cdot V_{sup}} \tag{7.1}$$

où f_s est la fréquence d'échantillonnage, L_{min} est la longueur minimale, SNR est Le rapport signal sur bruit, V_{sup} est l'alimentation, et P_{dis} est la puissance dissipée. La Figure 7.1 montre FOM versus la marge dynamique(DR).

Premièrement, cette figure montre la validation de l'architecture du convertisseurs A/N proposé entre les convertisseurs A/N à haute résolution. Deuxièmement, les performan-

ces du convertisseur A/N proposé sont meilleures ou comparables à celles d'autres architectures de convertisseurs de 10-bit à 11-bit. Troisièmement, la figure montre un grand potentiel de l'architecture proposée pour concevoir des convertisseurs A/N à haute performances en mode courant. La Figure 7.1 montre aussi que les convertisseurs A/N dans [13] et [20] ont des performances meilleures grâce à leur faible dissipation de puissance. Donc, le convertisseur A/N en mode courant proposé peut être un bon candidat pour les convertisseurs à haute résolution si sa dissipation de puissance est minimisée.

Quant au test, la contribution consiste en la conception d'un circuit d'auto test (BIST). Le circuit BIST a été conçu pour tester le INL, le DNL, l'erreur de gain et l'erreur de décalage d'un convertisseur analogique/numérique. Le test a été fait dans le domaine digital, ce qui élimine la nécessité de calibrer le circuit. Le circuit principal utilisé dans le BIST est un convertisseur numérique-analogique N/A souvent utilisé dans la majorité des convertisseurs A/N. Le circuit BIST proposé est généralement utilisé dans des convertisseurs A/N en pipeline de grande résolution. Ceci est dû au fait que l'on peut tester un convertisseur A/N en pipeline en testant seulement le dernier étage. Il a été montré que le BIST peut utiliser le même convertisseur N/A que celui en pipeline. Par conséquent, ce BIST peut donner une bonne couverture de pannes pour les convertisseurs A/N en pipeline. Donc, la résolution, la surface additionnelle, le temps de test et la précision peuvent être améliorés de façon significative. Normalement, la source d'erreurs principale dans n'importe quel convertisseur A/N est reliée aux comparateurs, aux amplificateurs, aux tensions de référence et aux convertisseurs N/A utilisés. Ce BIST n'est pas basé sur un modèle de pannes spécifique du circuit dans le convertisseurs A/N.

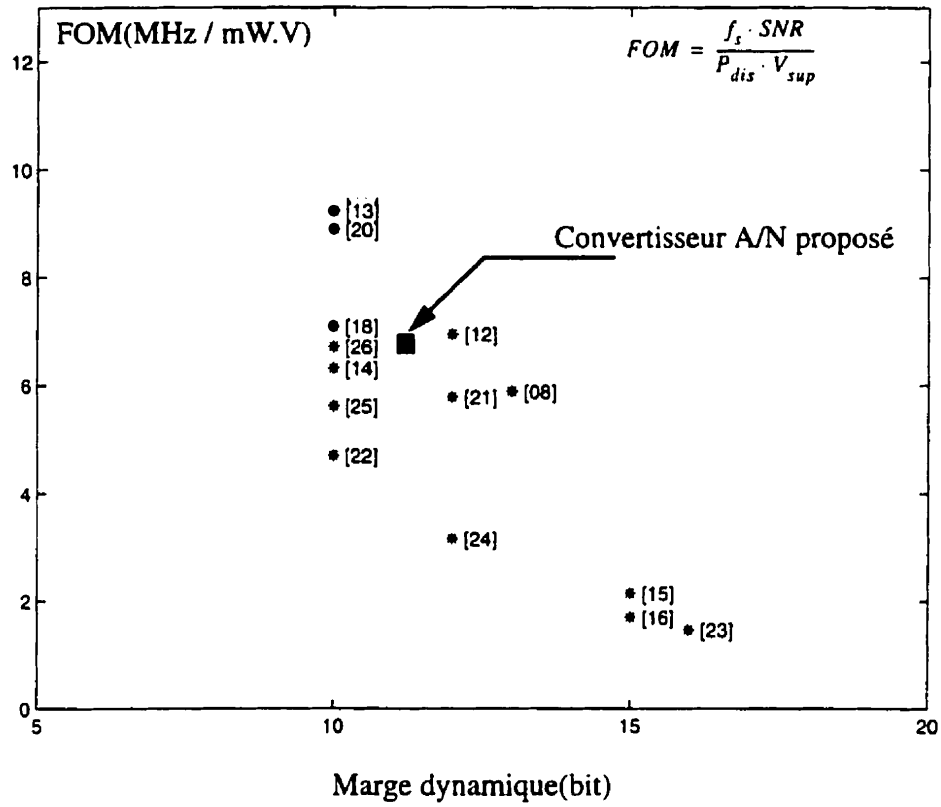

Figure 7.1 Convertisseur A/N proposé comparé aux architectures les plus récentes mentionnées dans le Chapitre 2.

7.2 Aperçu sur les travaux de recherche futures

Comme l'échelle de la technologie CMOS continue à être réduite, les circuits numériques vont augmenter leurs avantages en termes de vitesse, de puissance et de surface consommée. Ces avantages se transposent difficilement aux circuits analogiques. Le convertisseur A/N est devenu un composant de base dans les circuits DSP ou les systèmes de communication. Par conséquent, il est essentiel d'étudier comment la réduction d'échelle de la technologie peut affecter les performances d'un circuit mixte, tels que le convertisseur A/N. Les exigences futures des interfaces à base de circuit analogique utilisés dans les systèmes DSP sont la minimisation du coût, l'augmentation de la vitesse de fonctionnement et la minimisation de la tension d'alimentation.

Le procédé de fabrication actuellement utilisé pour les circuits en mode courant est le même que celui utilisé pour les circuits numériques. Cependant, la baisse des coûts des circuits analogiques dépend de notre capacité de développer de nouvelles techniques de conception qui sont compatibles avec les nouveaux procédés de fabrication des circuits numériques.

Actuellement, les circuits en mode courant ne peuvent pas être utilisés dans des applications de haute fréquence tels que le traitement numérique des signaux vidéo. Pour arriver à cette fin, des techniques de conception de circuit en mode courant doivent être développées pour être compatibles avec le nouveau procédé de fabrication sub-micronique pour augmenter la largeur de bande des transistors MOS

Les circuits en mode courant actuels ne peuvent pas fonctionner avec des tensions d'alimentation inférieures à 3 V. L'industrie a proposé de baisser encore plus la tension d'alimentation à 2.4 V ou même à 1.8 V, pour la prochaine génération des circuits VLSI. En conséquence, pour la prochaine génération des systèmes DSP, les techniques basées sur le mode courant doivent être améliorées pour ne pas dégrader la performance des circuits alimentés avec des tensions faibles.

En conclusion, en utilisant des architectures et des techniques de conception de circuits combinées à une technologie à petite échelle, un convertisseur A/D de grande vitesse fonctionnant à faible tension et à faible puissance peut être réalisé. La prochaine étape dans ce projet est d'examiner les effets d'intégration d'un tel convertisseur comme un bloc dans un système complexe et de résoudre les problèmes d'intégration, comme le bruit de couplage du substrat, le bruit de commutation dans les alimentations, etc...

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ANNEXE

Circuits Description

A.1 Voltage Mode Comparator

Figure A.1 shows the comparator circuit, which consists of a preamplifier(M1-M2 and Q1-Q4), offset storage capacitor(C1-C2), a bipolar latch(Q5-Q6 and M11-M12), and a CMOS latch (M3-M10). It is controlled by two clocks, $\phi 1$ and $\phi 2$. The circuit operates as follows. In the calibration modes, S1 and S2 are off and S3-S6 are on, thereby grounding the inputs of the preamplifiers and the bipolar latch. The preamplifier input offset is thus amplified and stored on C1 and C2. In this mode, the two latches are also reset. In the comparison mode, first S3-S6 turn off while S1 and S2 turn on; the input differential voltage is sensed and amplified, generating a differential voltage at the bipolar latch input. Next, the two latches are strobed sequentially to produce the output.

A.1.1 Preamplifier

The preamplifier circuit is shown in Figure A.1. It comprises source followers M1 and M2, the differential pair Q1 and Q2, and emitter follower Q3 and Q4. As temperature increases, the gate-source voltage of M1 and M2 increases but the base-emitter voltage of Q1 and Q2 decreases. The input voltage range is therefore relatively constant with temperature.

An important issue in preamplifier design is the input noise. The flicker noise of MOS devices is quite substantial; as a consequence, large transistors must be used at input.

However, this noise can be effectively removed by an offset cancellation operation. If the comparator performs calibration in every cycle, the time interval between offset cancellation and comparison does not exceed a few tens of nanoseconds.

Hence, only those flicker noise components that change appreciably in this time interval will be significant. Due to the 1/f dependence of flicker noise, these components have very small magnitudes and thus are negligible. As a result, the source follower dimensions are dictated only by thermal noise requirements. The preamplifier input-referred noise per unit bandwidth is given by Eq. 3.9.

Emitter follower Q3 and Q4 buffer the outputs and, together with D1 and D2, shift the output voltage down to establish a bias across capacitor C1 and C2, which are simply large NMOS transistors in this design.

A.1.2 Bipolar Latch

The bipolar latch, shown in Figure A.1, consists of cross-coupled devices Q5 and Q6, and a charge-pumping circuit, M11, M12, nad C3. The coupling capacitors C1 and C2 act as both offset storage elements and load devices for the bipolar latch. During calibration, $\Phi 1$ is low, grounding the nodes X1 and Y1, and $\Phi 2$ is high, discharging C3 to V_{EE}. During comparison, $\Phi 1$ goes high and, after the preamplifier has sensed the input and a differential voltage is developed at X1 and Y1, $\Phi 2$ goes low, turning Q5 on and transferring charge through the bipolar pair. Then, the voltage difference between nodes X1 and Y1 is regeneratively amplified until C3 charges up and the tail current falls to zero. This operation, which can be viewed as charge-sharing between C3 and the combination of C1 and C2, occurs quickly because of positive feedback around Q5 and Q6 and the large transconducatnce of these devices.

The main advantage of this bipolar latch is to have zero static power dissipation. Also, in this comparator, the preamplifier needs only attenuate the input offset resulting from the V_{BE} mismatch of the two bipolar transistors Q5 and Q6, rather than the larger V_{GS} mismatch of two MOS devices as would be necessary if a CMOS latch were used.

A.1.3 CMOS Latch

The last stage of the comparator is a CMOS latch, shown in Figure A.1, that is used to generate CMOS levels from the output of the bipolar latch. It consists of sense transistors M3 and M4, cross-coupled devices M5-M8, reset transistors M9 and M10, and a CMOS clock delay inverter G1. The operation of this latch is based on charge-sharing between C1 and the capacitance at the node X2, and between C2 and the capacitance at the node Y2. In the calibration mode, when Φ2 is high, M3 and M4 are off, and M9 and M10 discharge X2 and Y2 to V_{EE}. In the comparison mode, Φ2 goes low to strobe the bipolar latch and turn off M9 and M10. Then, following a delay controlled by C3, transistors M3 and M4 turn on, coupling the voltage difference between X1 and Y1 to the sources of M5 and M6 and initiating regeneration at nodes X2 and Y2. The regeneration continues until either X2 or Y2 reach the voltage at X1 or Y1, while the other has returned to VEE. In order to have fast response, this latch must be designed with short-channel devices. This in turn results a high offset voltage. Therefore, this latch must be strobed only after the bipolar latch has generated a sufficient differential voltage at X1 and Y1. This is accomplished by setting the switching point of G1 above -2.5 V, so that its output does not go low until C3 has charged up by at least 2 Volts. In order to prevent degradation of X1 and Y1 common-mode voltage, M3 and M4, which remains on as long as Φ2 is low, are followed by cross-coupled devices M5 and M6

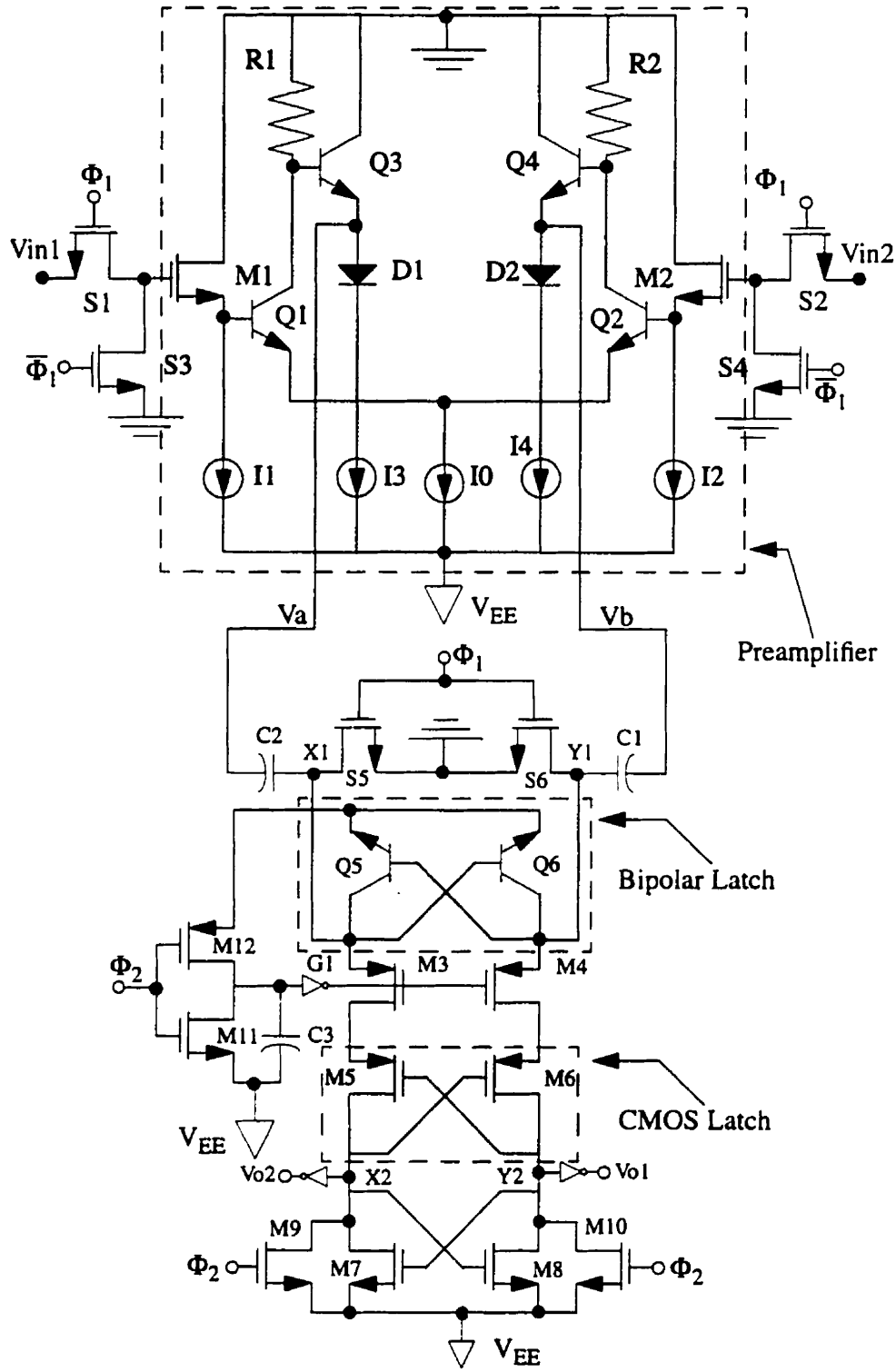

Figure A.1 Schematic of voltage mode comparator.

A.2 BiCMOS Operational Amplifier

The performance of subtracter used in subranging A/D converter mainly depends on the performance of operational amplifier. The key design goals are high GBW, high DC gain, enough swing voltage and low power dissipation. The first choice is use of simple differential amplifier with active load. The main disadvantage of the simple differential pair with active load structure is the limited output voltage swing. To overcome this problem, two extra current mirrors are usually added to the simple one. Although, the swing is increased a little but the GBW is missed. To compensate the problem of the reduction in the GBW due to extra current mirror, a cascode structure can be used. To overcome the problem of long settling time the technique of feedforward compensation has been used. Figure A.2 shows a complete schematic of designed operational amplifier. The full description of this circuit including its analysis has been explained in *Analog Integrated Circuits and Signal Processing, Kluwer Publishing, Vol. 11, No. 1 , pp. 63-71, 1996.*

As shown in Figure A.2, this circuit consists of four parts; biasing circuit, folded-cascode amplifier, feedforward compensation network and common-mode feedback network. Transistors Q1-Q2, M3-M6, and Q7-Q8 form a folded-cascade amplifier, combined with a common-mode feedback network(CMFC), M11-M14. The CMFC senses the change in the common mode output level and creates a a proportional voltage which will be feedback to M9 and M10 to change the bias current and hence the output's common mode voltage. The compensation network consists of R_f and C_f. Transistors M15-M24 form the bias circuit which generate the required DC voltages in the amplifier.

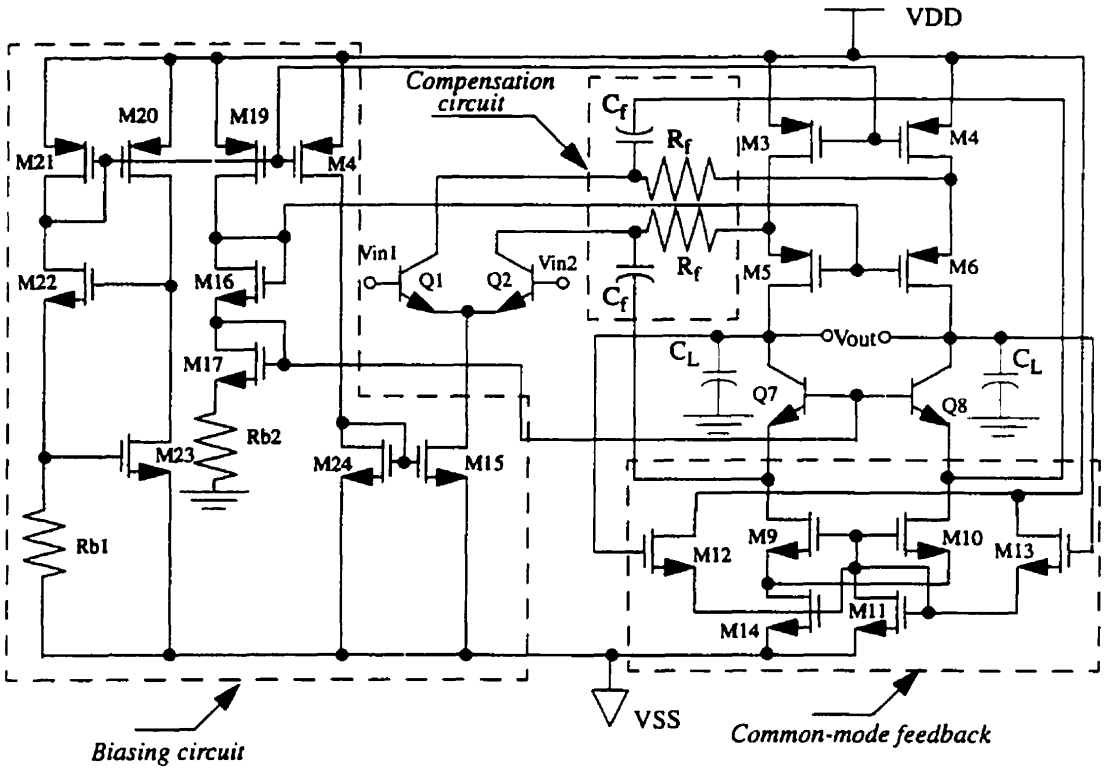

Figure A.2 Schematic of BiCMOS operational amplifier.

A.2.1 BiCMOS Op-Amp without Compensation

The CMOS cascode op-amp with single-ended output suffers from a number of trade-offs among its gain, dynamic range, slew rate, and settling time. To relieve some of these problems, a fully differential structure can be used. In this circuit, signal do not propagate through PMOS devices. This circuit still suffers from the same dynamic range trade-off mentioned for single-ended output circuit. In order to increase the input and output swing, the cascode topology can be folded, as illustrated in Figure A.3. Here, PMOS devices M5 and M6 are in the signal path, creating a non-dominate pole at the folding points X and Y. This pole depends on the transconductance of M5 and M6 and the total capacitance at these nodes. This pole usually determines the phase margin and GBW of the op-amp. In

this circuit, the bipolar transistors, Q7 and Q8, will increase the non-dominate pole. The DC gain of operation amplifier will be provided by bipolar transistor Q1 and Q2, as shown in Figure A.3.

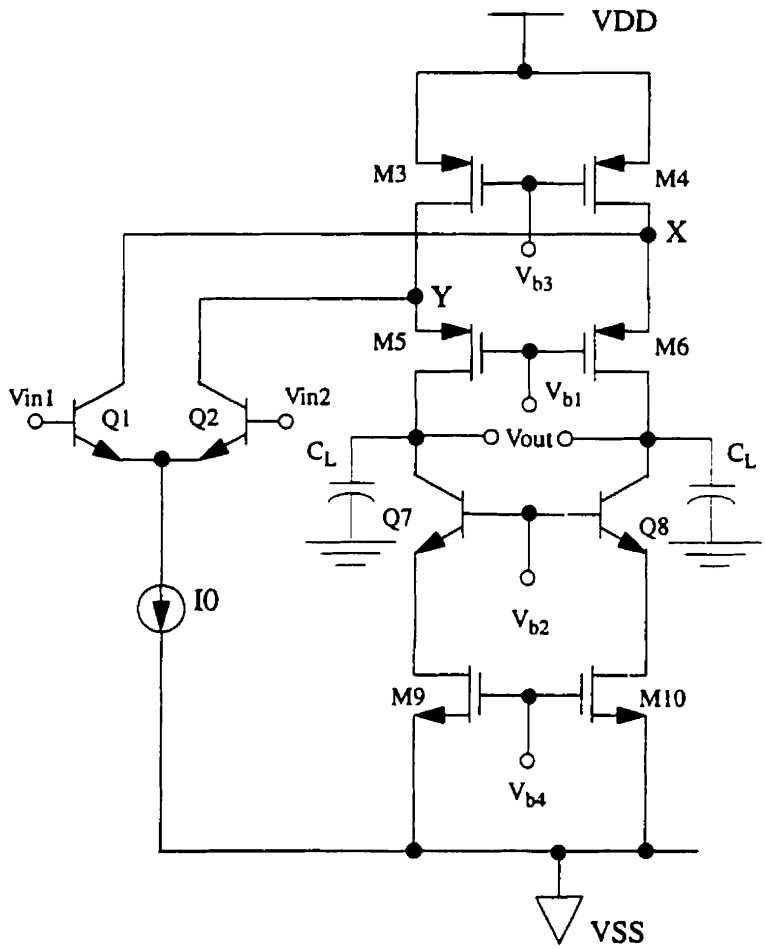

Figure A.3 BiCMOS Folded cascode amplifier without compensation.

A.2.2 BiCMOS Op-Amp with Feedforward Compensation

The DC gain has been provided by using bipolar transistors in input stage. However, it inevitably have PMOS devices in the signal path, thus suffering from a significant non-dominate pole and hence long settling time. This non-dominate pole at node X is given by

$$f_2 = \frac{1}{2\pi} \frac{g_{m6}}{C_{gs6} + C_{gd4} + C_{db4} + C_{sb6} + C_{\mu 1} + C_{cb1}} \tag{A.1}$$

which is roughly a factor two higher than the usual current mirror structure. As a result a gain in phase margin of 10°-15° is obtained.

It is clear that the maximum GBW depends on the slowest devices, in this circuit M6. The technique of conventional feedforward is used to overcome the limit of GBW. This technique is shown in Figure A.4. The high frequency signal is flowing through C_f and passing-by M6 transistor. The second non-dominate pole in the compensated circuit is given by

$$f_2 = \frac{1}{2\pi} \frac{g_{m8}}{C_{gs10} + C_{db10} + C_{eb8} + C_{\pi 8} + C_{\mu 1} + C_{cb1}} \tag{A.2}$$

Now, this term can be maximized by Q8 parameters, without affecting other parameters. It is also clear that g_{m8} in bipolar technology is much bigger than in CMOS. Thus, this also increases f_2. The GBW in this circuit is given by

$$GBW_{max} = \frac{f_2}{2} \tag{A.3}$$

In this design, the second pole without feedforward compensation is 300 MHz. After feedforward compensation, it increases to 1.7 GHz.

The effect of C_f can be explained by calculating the step response of Figure A.4. The step response of an amplifier with the low frequency open loop gain(A), the zero and the pole(f_Z , f_P) before the GBW, and the applied step input voltage(V_{step}), is given by :

$$V_{out(t)} = V_{step}\left[1 - \frac{A}{A+1}\exp(-2\pi GBWt) + y\right] \tag{A.4}$$

where y is

$$y = \frac{f_Z - f_P}{GBW}\exp\left(-2\pi f_Z t\right) \tag{A.5}$$

The y term must be decreased in order to improve the step response. The pole and zero in Eq. A.4 are given by:

$$f_p = \frac{1}{2\pi C_f R_f\left(1 + \frac{C_1}{C_f} + \frac{C_1}{C_L}\right)} \tag{A.6}$$

$$f_z = \frac{1}{2\pi C_f R_f} \tag{A.7}$$

where C_1 is the total capacitance at collector node of Q1 and C_L is the load capacitance.

Normally, the third term in Eq. B.6 can be ignored($C_L >> C_1$). Eq. B.4 and Eq. B.5 show that the step response of folded-cascode amplifier can be independent of load capacitance if C_L is large enough, CL>1 pF. On the other hand, for a good response, C_f should be larger than C_1. The simulation results show that the settling time is improved by 80% for $C_f = 1pF$ compared in op-amp without compensation circuit.

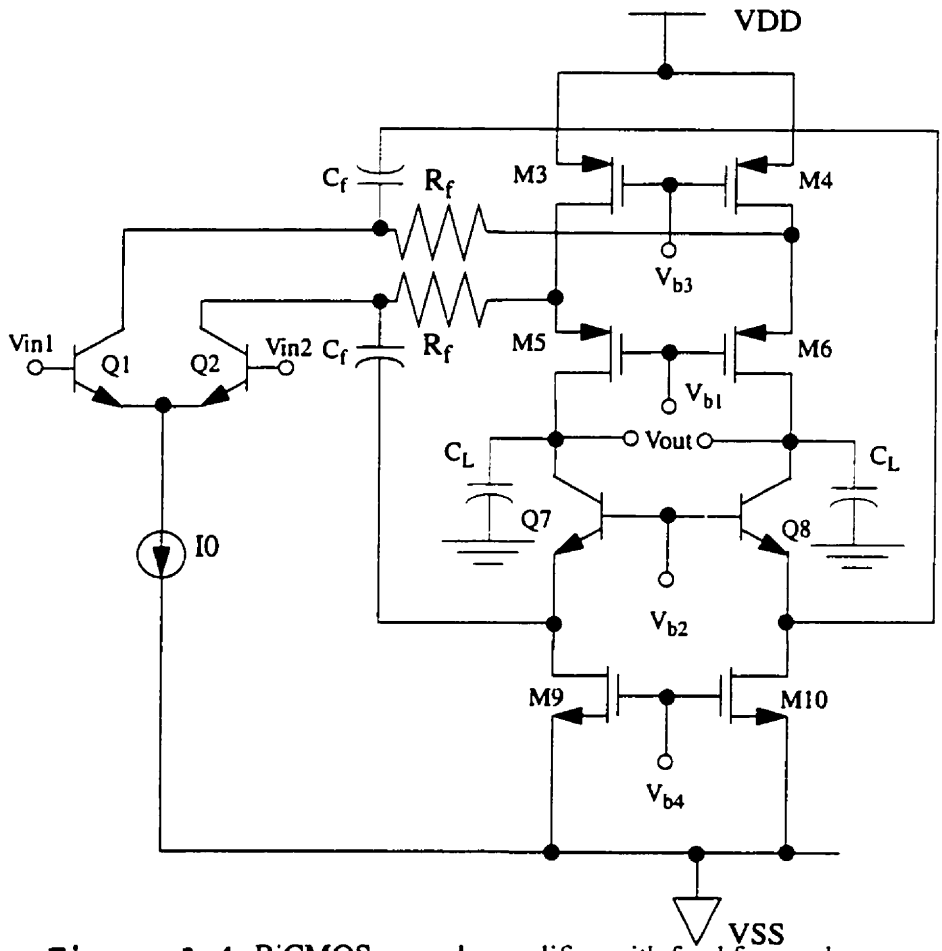

Figure A.4 BiCMOS cascode amplifier with feed forward compensation.

A.2.3 Common-Mode Feedback

In high-gain, fully differential op-amps, the output common-mode(CM) level must be well defined if the circuit is used in closed loop form. In practice, common-mode variations may introduce long settling times in the differential output. The principal issue in the design of common-mode feedback circuit(CMFC) is that it can sense the CM output voltage but not the differential mode(DM) output voltage. The output signal of the CMFC is fed back to the amplifier to adjust the DC current in the output stage so that CM output voltage can be maintained at a DC level, normally at zero.

This op-amp uses a simple circuit as shown in Figure A.4 where transistors M11-M13 provide common-mode feedback. In this circuit, M12 and M13 sense the output voltage and produce a common-mode level in the output. The drain current in M14 is based on the applied voltage to M11. The current in M14 fixes the common-mode voltage at V_{GS12} + V_{GS13}. For small differential swing at output, the current in the drain of M11 is constant and the CM level is fixed. However, for a large differential variation, as M12 begins to turn off, the gate voltage of M11 rises, increasing I_{D14}. The change in I_{D14} is drawn from M9 and M10, but not equally, because these transistors have slightly different g_m. Therefore, a asymmetric component appears at the output. This component can increases the settling time of the BiCMOS op-amp. The Simulation result shows that settling time of BiCMOS op-amp is improved by using CMFC. The settling time without CMFC is about 8 nsec. The settling time with CMFC is about 4 nsec. The degrading of the settling time with CMFC is because of CMFC weak response in large differential output

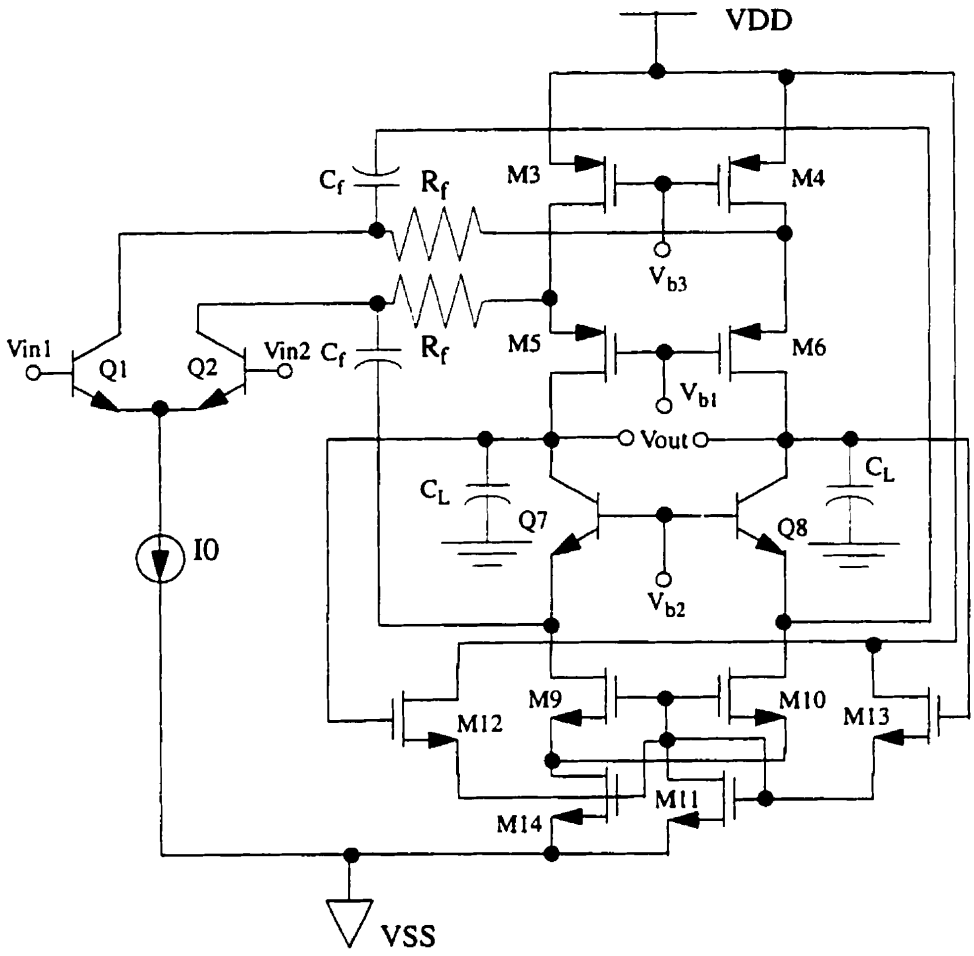

Figure A.5 BiCMOS cascode amplifier with compensation and common-mode feedback.

A.3 Current Mode Switch

The current mode switch, shown in Figure A.6, consists of four units; write unit, read unit, switch unit, and controlled bias unit. The write unit consists of two transistors; M_W and M_{B1}. Transistor M_W operates in saturation mode and acts as a diode. Therefore, its input shows low resistance which is suitable for input current. Transistor M_{B1} is controlled by transistor MC6 which in turn controlled by external digital signal. The input current signal will be stored as a charge in the gate capacitance of M_W.

The current read unit consists of two transistors M_R and M_{B2}. Transistor M_{B2}, which is controlled by transistor MC6, provides enough current so that M_R is always in saturation.

The switch unit uses two conventional MOS switch as shown in Figure A.6. M_{S1} is for connecting the stored charge in the write unit to the input of the read unit. The other transistor, M_{S2}, is used to ground the read input when the current switch is off. Both transistors in the switch unit are controlled by an external digital signal which is generated by the logic unit.

The controlled bias unit current consists of M_{C1}-M_{C6}. Transistors M_{C1}-M_{C5} form a current source which provides enough current for the read and write transistors to be in saturation. In addition, the DC current of this current source is controlled by an analog external signal. This control will be used to set the current switch when the input current is zero. Moreover, when the current switch is off, Mc6 will turn on. Therefore, M_{B1} and M_{B2} will turn off. This causes to reduce power dissipation during off mode of current switch.

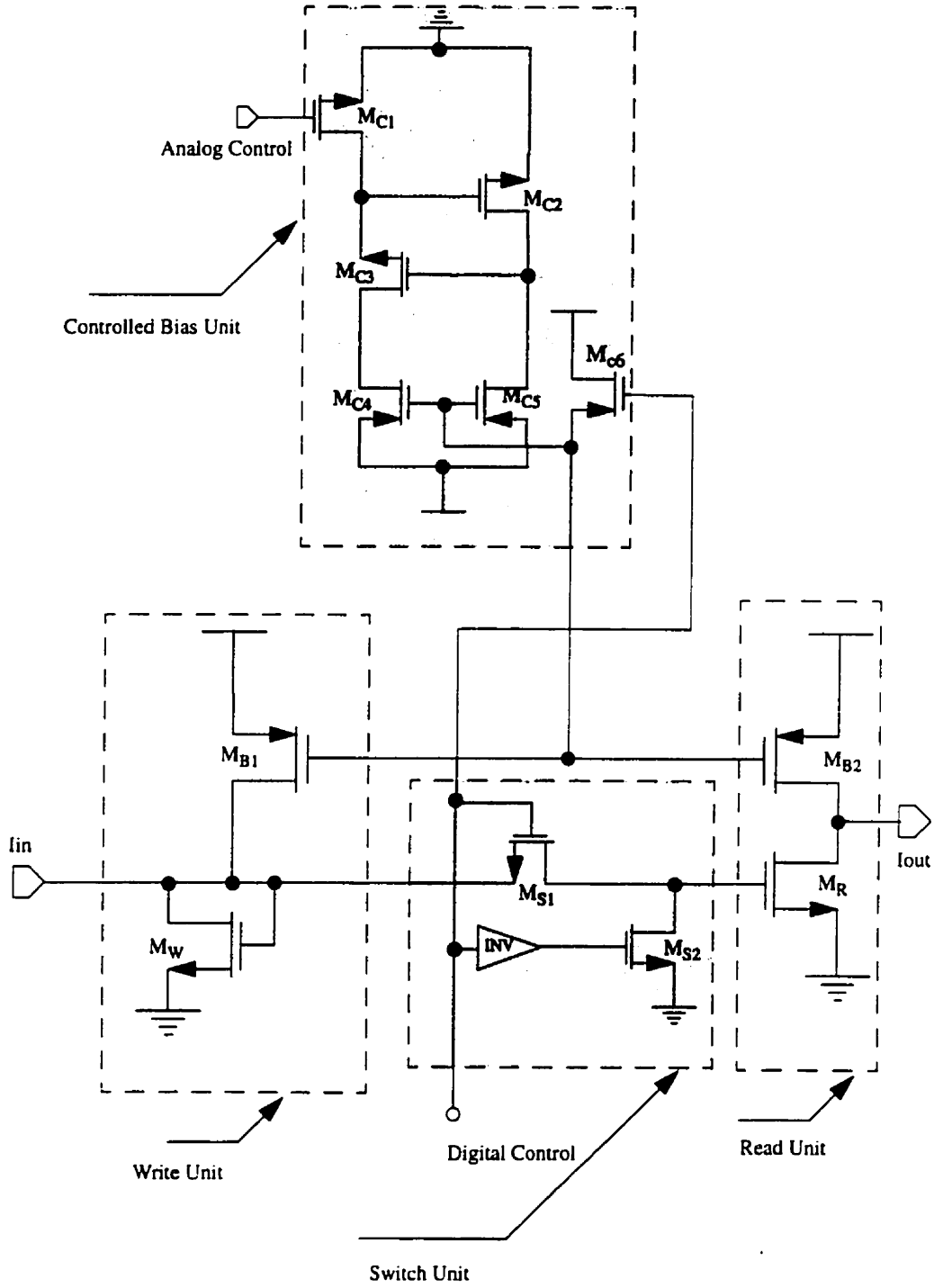

Figure A.6 Schematic of current mode switch.

A.4 Current Mode Comparator

Figure A.7 shows the schematic of the proposed current comparator. It consists of an inverter and a CMOS buffer. When the clock set at high, the comparator is inactive and its positive output is low. When the clock set at low, the comparator output is active and its voltage depends on the current input. The switches between the comparator and output inverters make the comparator operates with the clock.

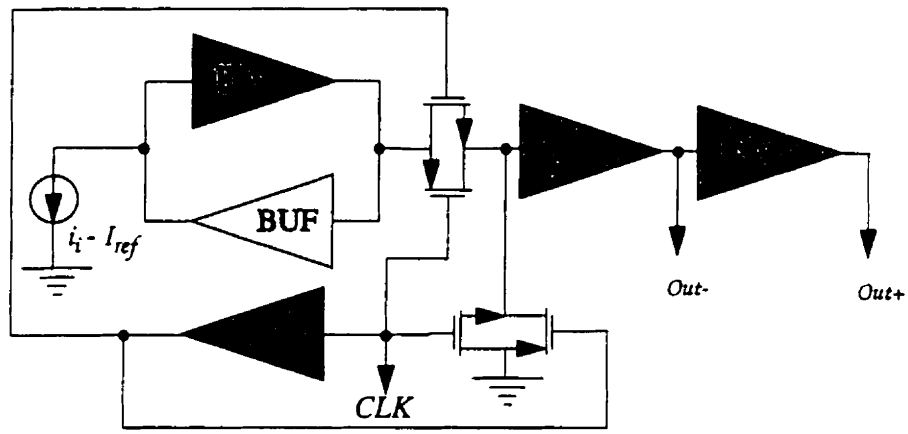

Figure A.7 Schematic of CMOS current comparator.

Figure A.8 shows the circuit of inverter and buffer. The inverter consists of M1-M2 and the buffer consists of M3-M4.

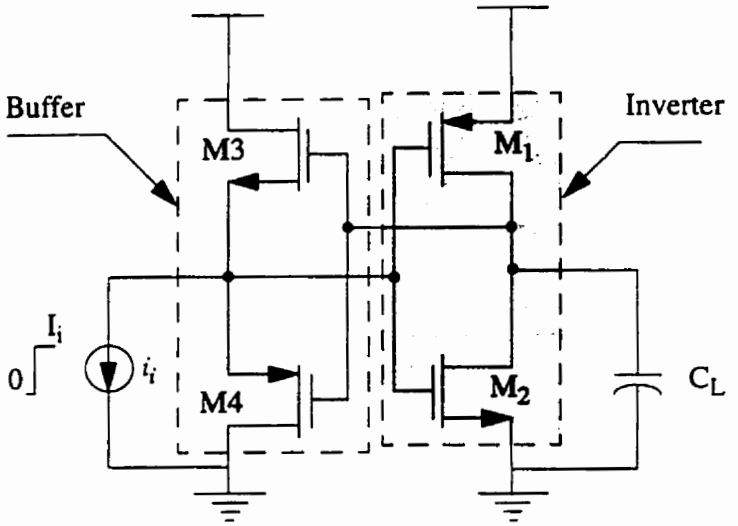

Figure A.8 CMOS current comparator with buffered.